| RGPV (DIPLOMA WING) BHOPAL | OBE CURRICULUM FOR THE COURSE | FORMAT-3 | Sheet No. 1/5 |
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| Branch | OPTOELECTONICS | Semester | 3 |
|---|---|---|---|
| Course Code | | Course Name | Digital Electronics |

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| **Course Outcome 1** | Examine the structure of various number system, codes and logic gates. | Teach Hrs | Marks |
| **Learning Outcome 1** | List out different types of number system & code and convert one to another. *(Cognitive)* | 5 | 6 |
| **Contents** | **Number System:**<br>Decimal number, binary number, octal and Hexadecimal number.<br>**Binary Codes:**<br>Weighted and un-weighted codes BCD, Gray, Excess-3.<br>**Conversion of number system and code:**<br>(Decimal number, binary number, octal and Hexadecimal number, BCD, Gray, Excess-3) | | |
| **Method of Assessment** | External | | |
| **Learning Outcome 2** | Perform various binary arithmetic operation. *(Cognitive)* | 3 | 6 |
| **Contents** | **Binary operations:**<br>Binaryaddition,subtraction, Multiplication, Division.<br>**Complement of number:**<br>Complements:1's,2's,9'sand10's.<br>Subtraction using 1's and2's complement. | | |
| **Method of Assessment** | Internal | | |
| **Learning Outcome 3** | Verify truth table of all the gates. *(Psychomotor)* | 4 | 8 |
| **Contents** | **Logic Gates:**<br>Symbol, operation and truth-table:<br>AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR<br>Realization of logic gates using universal gates.<br>**Logic System:**<br>Positive and negative logic system.<br><br>Verification of the basic logic gates (AND, OR,NOT NAND , NOR ,EX-OR and EX-NOR). | | |
| **Method of Assessment** | External | | |

| RGPV (DIPLOMA WING) BHOPAL | OBE CURRICULUM FOR THE COURSE | FORMAT-3 | Sheet No. 2/5 |
|---|---|---|---|

| Branch | OPTOELECTONICS | Semester | 3 |
|---|---|---|---|
| Course Code | | Course Name | Digital Electronics |

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| **Course Outcome 2** | Construct and Examine simple combinational digital circuit. | Teach Hrs | Marks |
| **Learning Outcome 4** | Explain Boolean algebra laws and theorems.*(Psychomotor)* | 4 | 5 |
| **Contents** | **Laws and theorems of Boolean algebra:**<br>Boolean laws, De-Morgan's Theorem and Duality Theorem, Complement of Boolean equations.<br>Verification of De- Morgan's theorem. | | |
| **Method of Assessment** | Internal | | |
| **Learning Outcome 5** | Solve Boolean expressions using K-map and realize its logic circuit. *(Cognitive)* | 6 | 5 |
| **Contents** | **Karnaugh-map:**<br>Boolean expressions: Sum of product and product of sum, Karnaugh maps and its use forsimplification up to four variable Boolean expressions, Don't care condition.<br>**Realization of logic equations:**<br>The universal building blocks-NAND & NOR, AND-OR network, NAND-NAND Logic for implementation of Boolean expressions. | | |
| **Method of Assessment** | External | | |
| **Learning Outcome 6** | Implement different type of adder and subtractor circuits. *(Cognitive)* | 4 | 5 |
| **Contents** | **Adder and Subtractor Circuit:**<br>Half adder, full adder, parallel binary adder, 8421 adder, half subtractor, full subtractor, parallel binary subtractor. | | |
| **Method of Assessment** | External | | |
| **Learning Outcome 7** | Design different type of coder and multiplexer circuits *(Psychomotor)* | 6 | 5 |
| **Contents** | **Coder Circuit:**<br>Encoder, Decoder<br>(2 to 4 line,3 to 8 line, BCD to Decimal, Decimal to7 segment)<br>**MUX Circuit:**<br>Multiplexers: 4 to1 and 8 to1.<br>De-Multiplexers: 1 to 4 and 1 to 8.<br>(Block Diagram and Truth table)<br>Verification of encoder, decoder, multiplexer and de-multiplexer circuit. | | |
| **Method of Assessment** | Internal | | |

| RGPV (DIPLOMA WING) BHOPAL | OBE CURRICULUM FOR THE COURSE | FORMAT-3 | Sheet No. 3/5 |
|---|---|---|---|

| Branch | OPTOELECTONICS | Semester | 3 |
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| Course Code | | Course Name | Digital Electronics |

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| **Course Outcome 3** | Analyze flip-flop circuit, counters, shift registers and understand their operation. | Teach Hrs. | Marks |
| **Learning Outcome 8** | Analyze the working of various flip-flops and verify its outputs. *(Psychomotor)* | 4 | 8 |
| **Contents** | **Flip-Flop:**<br>S-R flip-flops(FF), D FF, Types of Triggering, Glitch,<br>JK FF race around condition and remedies,<br>JK Master Slave FF and T FF.<br>Verification of various flip-flops | | |
| **Method of Assessment** | Internal | | |
| **Learning Outcome 9** | Draw and explain different type of registers. *(Cognitive)* | 4 | 6 |
| **Contents** | **Registers:**<br>Shift Register (3 to 4 bits only)- introduction, circuitdiagram and waveforms of SISO, SIPO,PISO, PIPO shift registers. | | |
| **Method of Assessment** | External | | |
| **Learning Outcome 10** | Design different type of synchronous and asynchronous counters. *(Psychomotor)* | 4 | 6 |
| **Contents** | **Counters:**<br>Asynchronous:<br>Up/down counters, Up-down counters.<br>Synchronous Counters.<br>Up/down counters, Ring counter, Johnson counter.<br>Design Mode-4 counters. | | |
| **Method of Assessment** | External | | |

| RGPV (DIPLOMA WING) BHOPAL | OBE CURRICULUM FOR THE COURSE | FORMAT-3 | Sheet No. 4/5 |
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| Branch | OPTOELECTONICS | Semester | 3 |
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| Course Code | | Course Name | Digital Electronics |
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| **Course Outcome 4** | Demonstrate the functioning of A to D and D to A Converters. | Teach Hrs | Marks |
| **Learning Outcome 11** | Draw and explain various operation of D/A conversion circuits. *(Cognitive)* | 3 | 10 |
| **Contents** | **D/A Conversion**:<br>Weighted resister, R-2R ladder network. | | |
| **Method of Assessment** | Internal | | |
| **Learning Outcome 12** | Draw and explain various operation of D/A conversion circuits. *(Cognitive)* | 5 | 10 |
| **Contents** | **A/D Conversion:**<br>Counter type, Successive approximation, Flash type, Dual slope type.(Theoretical aspects) | | |
| **Method of Assessment** | External | | |

| RGPV (DIPLOMA WING) BHOPAL | OBE CURRICULUM FOR THE COURSE | FORMAT-3 | Sheet No. 5/5 |
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| Branch | OPTOELECTONICS | Semester | 3 |
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| Course Code | | Course Name | Digital Electronics |
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| Course Outcome 5 | Compare various digital logic family. | Teach Hrs. | Marks |
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| Learning Outcome 13 | Compare digital ICs on different parameters. *(Cognitive)* | 4 | 8 |
| Contents | **Characteristics of digital ICs:**<br>Fan-in, Fan-out, Propagation delay, Power dissipation, Noise margins, Figure of merit.<br>**Logic ICs:**<br>NAND Gate using TTL, NOR gate using ECL. | | |
| Method of Assessment | External | | |
| Learning Outcome 14 | Construct universal gates and inverter using MOS and CMOS logic. *(Cognitive)* | 4 | 6 |
| Contents | **Classifications of logic families:**<br>Saturated and Non-saturated logic.<br>**MOS and CMOS Logic:**<br>MOS based NOT gate, Two input NAND & NOR gate.<br>CMOS based NOT gate, Two input NAND & NOR gate. | | |
| Method of Assessment | External | | |
| Learning Outcome 15 | Make use of PAL & PLA for implementation of Boolean expression and design simple logic circuit. *(Cognitive/Affective)* | 4 | 6 |
| Contents | **PLD:**<br>PAL,PLA<br>Implementation of Boolean expression using PAL,PLA (Up-to 2 variables) | | |
| Method of Assessment | Internal | | |