OBE CURRICULUM FOR THE COURSE

Branch		Сог	nputer	Science and E	ngineering	Semester	1	Ι			
Course (Code			Course Name	Dig	gital Techniq	lue				
Course	Outc	ome 1	Perfo and b comp	rm conversion am ecame familiar wi uter.	ong different number th basic codes used ir	r systems, n digital	Teach Hrs.	Marks			
Learnin	ig Ou 1	tcome	Defin anoth	e signals and co er.(Cognitive)	nvert onenumber sys	stemsto	07	10			
Contents			Advantages and disadvantages of Digital Circuits. Number System-Introduction to binary, octal, decimal and hexadecimal number systems Conversion between number system.								
Met Asse	thod of the second s	of nt	Intern	nal							
Learnin	ng Ou 2	tcome	Expla arithr	ain differentcode netic.(Cognitive	s andperform binary	1	07	10			
Contents			Binary Arithmetic-Binary addition, subtraction, Multiplication and division. 1's and 2's complements and its utilization Codes-BCD, Grey Code, Excess 3, EBCDIC, ASCII Code and its uses								
Met Asse	thod o essme	of nt	Exter	nal							

OBE CURRICULUM FOR THE COURSE

Branch		Computer Science and EngineeringSemesterII											
Course (Code			Course Name	Dig	ital Techniq	ue						
Course	Outco	ome 2	Desig Boole	n simple Logic Circu an laws and rules c	uit with logic gates by on expression.	applying	Teach Hrs.	Marks					
Learnin	ng Ou 3	tcome	Draw expre	y symbol andwrite ession for allthe ga	truth table & logicantes.(Cognitive)	ıl	07	10					
Со	ntent	8	Logic Symb AND,0 OR,EX Realiz	Gates: Basic conce ols, Truth Table and OR,NOT Universal (C-NOR Cation of All Other (pts of Diode/transisto d Logical expression o Gates-NAND and NOF Gates Using Universa	or switch circo of Basic logic (Special Purp Gates	uit, Logic (gates- ose Gates	Gates S-EX-					
Met Asse	thod o	of nt	Exte	ernal									
Learnin	ng Ou 4	tcome	Solve map.	e equation using B (Cognitive)	oolean algebra and	K-	08	10					
Со	ntent	S	 Boolean Algebra-Rules and Laws of Boolean Algebra, De-Morgan's Theorem. Duality Theorem Introduction to logic design with Karnaugh map Simplification of Boolean Function up-to 4 variables(2,3,4 variable), Don't Care Condition Boolean Representation-Sum of Product and product of Sum, Min Term and Max torm 										
Me	thod o	of nt	Exter	mal									
Learnin	ig Ou 5	tcome	Imple and E	ement and verify t Boolean equation.	ruth table of given l (Psychomotor)	ogic gates	06	15					
Со	ntent	S	Verify truth table of NOT and, OR, EX-OR, EXNOR, NOR, NANDgates. Implement AND, OR and NOT gate using NOR and NAND gate and verifytruth table. Implement and verify truth table of De-Morgan's theorem. Implement simple Boolean equation using gates and verifyoutput.										
Met Asse	thod o essme	of nt	Interi	nal									

OBE CURRICULUM FOR THE COURSE

Sheet

RGP WIN	V (DI G) B	PLON HOPA	/IA L	FOR TH	E COURSE	FORMA	г.3	Sheet No. 3/5
Branch		Cor	nputei	Science and En	gineering	Semester		II
Course (ourse Code		Course Name	Digi	ital Techniq	ue		
Course	Outco	ome 3	Learn hardv the de	the minimization t vare requirements esign of Combinatio	echniques to simplify of digital circuit and u onal circuit.	the nderstand	Teach Hrs.	¹ Marks
Learnin	ng Ou 6	tcome	Desig circu	gn Adder, Subtrac its.(Cognitive)	tor. Encoder and De	coder	07	10
Co	ontent	8	Half a Half S Basics Basics	dder, Full adder ubtractor and Full of Encoder,Decim of Decoder,BCD -t	Subtractor al to BCD Encoder :o -Seven Segments Do	ecoder.		
Me Ass	thod o	of nt	Exter	mal				
Learnin	ng Ou 7	tcome	Expla and c	ain differenttypes ode convertor.(Ce	of multiplexers, dem o gnitive)	nultiplexers	07	10
Co	ntent	S	Multi Multi Code	plexer/Demultiplex plexer,1:4 Demultip Convertor-BCD to I	er-Applications of Mu plexer Binary (74184),Binary	lltiplexer and l	Demulti A)	plexer,4:1
Me Asse	thod o essme	of nt	Intern	nal				
Learnin	ng Ou 8	tcome	Imple circu (Psyc	ement and verify g its. chomotor)	given combinational	logic	06	20
Co	ontent	8	Imple Verify Desig Study	ment and verify tru v truth table of 4:1 I n and implement D of Code converter	uth table of Half & Full Multiplexer, 1:4 De-m ecoder(2:4) and Enco and BCD adder.	l adder, Half & ultiplexer der(4:2)	Full Su	btractor
Me Ass	thod o	of nt	Exter	mal				

OBE CURRICULUM FOR THE COURSE

FORMAT-	Sheet
3	No. 4/5

Branch	Co	mputer	Science and En	gineering	Semester	I	Ι
Course (Code		Course Name	Digi	ital Techniq	ue	
Course	Outcome 4	Obtai logics	n basic knowledge within integrated o	of logic families for ir circuit.	nplement	Teach Hrs	Marks
Learnin	g Outcome 9	Defir (Cog	ne digital integrate nitive)	d circuits.		07	10
Со	ntents	Introc Chara	luction to Digital In cteristics of Digital	tegrated Circuits IC's			
Me Asse	thod of essment	Intern	nal				
Learnin	g Outcome 10	Com famil	pare the character ies.(Cognitive)	istics of different log	gic	08	10
Со	ntents	Chara Propa logic Analy	cteristics of Logic F gation delay Time Families –RTL, DTL, sis of open collecto	amilies –Power Dissi IIL, ECL, MOS or and tri –state Logic	pation, Speed	l, Fan in Fa	an Out,
Me Asse	thod of essment	Exter	nal				

OBE CURRICULUM FOR THE COURSE

FORMAT-3

Branch		Co	mputer	iter Science and Engineering Semester									
Course (Code			Course Name	Digi	tal Techniq	ue						
Course	Outco	ome 5	Under Flop, f	rstand the design o Registers and Coun	f Sequential Circuits su ters.	ich as Flip	Teach Hrs	Marks					
Learnir	ng Ou 11	tcome	Draw itsope	circuit ofdifferent eration.(Cognitive	t flip-flopsand explai	n	06	10					
Co	ontent	5	One-b Flip Fl Applic	it Memory Cell, Co op –S-R, Clocked R- ation of Flip Flop	ncept of clock Signal S, JK, JK Master Slave,	T and D Flip I	-lop,						
Me Ass	ethod o essme	of nt	Exter	nal									
Learnir	ng Out 12	tcome	Explain different types of shift register and counter. 06 10 (Cognitive)										
Co	ontent	5	Registers, Shift Register, types of Shift Register-SISO, SIPO, PISO, PIPO Counters-Basics of counter and its applications										
Me Ass	ethod o essme	of nt	External										
Learnir	ng Out 13	tcome	Desigr verify	n and Implement gi it.(Psychomotor)	ven SequentialLogic C	ircuits and	08	15					
Co	ontent	5	Verify truth table of RS, JK, D and T flip-flop. Design and Implement Shift registers using D flip-flop Design and Implement ripple counter using J-K flip-flop Design and Implement synchronous counter using J-K flip-flops.										
Me	ethod o essme	of nt	Intern	nal		- ·	-						

SuggestedListofExperiments:

S.No	Experiment list
1.	Study and Verify the truth table of logic gates (74xx series).
2.	Realization of AND, OR, NOT and Ex-OR logic gates using NAND and NOR gate
3.	Verification of De-Morgan's theorem
4.	Implement simple Boolean equation using gates and verifyoutput.
5.	Implement and verify truth table of Half and Full adder.
6.	Implement and Verify truth table of Half and Full Subtractor
7.	Study and Verify truth table of 4:1 Multiplexer
8.	Study and Verify truth table of 1:4 De-Multiplexer
9.	Design and implement 2:4 Decoder.
10.	Design and implement 4:2 Encoder.
11.	Study of gray to binary code convertor using gates
12.	Study of BCD adder
13.	Verification of truth table of RS, JK, D and Tflip flop using IC's.
14.	Design and ImplementShift registers using D flip-flop
15.	Design and Implement ripple counter using J-K flip-flop
16.	Design and Implement synchronous counter using J-K flip-flops.

ReferenceBooks/WebPortals:

1.	
2.	
3.	
4.	
5.	
6.	
7.	

	RGPV (Diploma Wing) Bhopal	SCHEME F	OR LEARNING	E	Branch Co	ode	Course C	ourse Code CO LO Code Cod		LO Code	Л		
KGPV	י (טוףוט)	oma wing j bi	nopai	OU	ТСОМЕ	С	0	2	0		1	1	Format No. 4
COURS	E NAME	Digital Technique	е										
CO Des	cription	Perform conversion	among d	ifferent number syster	ns, and became familiar with	n basi	c code	s used in dig	ital co	mpute	r.		
LO Des	cription	Define signals and	convert	onenumber systemsto	another								
					SCHEME OF STUDY								
S. No. Learning Content				Teaching – Learning Method	Description of T-L Process	Te F	each Irs.	Pract. /Tut Hrs	LRs Required			Remarks	
LO-01	LO-01 Definition of Signal, Comparisons Between Analog and Digital signal. Advantages and disadvantages of Digital Circuits. Number System-Introduction to binary, octal, decimal and hexadecimal number systems Conversion between number system		ns Ir nal. cl of P o mber	nteractive lassroom lecture, PT, demonstration, uiz, assignments	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/ assignments/ tutorial.		07		Text Boo Handout: board, ch lectures- others		Text Books, PPT, Handouts, chalk board, charts.Videos lectures- NPTEL& others		
	, ,			SC	HEME OF ASSESSMENT			1					
S. No.	Metho	d of Assessment		Description	of Assessment		Μ	aximum Marks	Res	ource	s Requ	iired	External / Internal
LO-01	LO-01 Mid Semester Theory Exam 2. Co 3. Do 4. Si			nt will be asked to(out various advant tal circuits. npare analog and d ine number system ple numerical on co	and/or): ages and disadvantages igital signal. and give example of ea onversion of number sys	of ch stem		10	Question paper, Rating scale			Internal	
	1		A	DDITIONAL INSTRU	ICTIONS FOR THE HOD/	FAC	ULTY	(IF ANY)					1

	RGPV (Diploma Wing) Bhopal	SCHEME	FOR LEARNING		Branch	n Code	Course Code C			CO Code	LO Code			
KGPV	י (טוקוט)	oma wing) Бп	opai	OL	JTCOME	С	(7	2	0		1	2	Format No. 4
COURS	E NAME	Digital Technique												
CO Des	cription	Perform conversion a	nong di	fferent number syste	ems, and became familiar wit	h basi	ic co	des used	in digi	tal cor	npute	er.		
LO Des	cription	Explain differentcoc	es and	perform binaryarith	nmetic									
					SCHEME OF STUDY									
S. No.	Le	earning Content	L	Teaching – earning Method	Description of T-L Pro	cess		Teach Hrs.	I	Pract /Tut Hrs.	•	LRs F	Requir	ed Remarks
LO-02	Binary Ari subtractic division. 1 and its uti Codes-BC EBCDIC, A	thmetic-Binary addition on, Multiplication and I's and 2's complement ilization D, Grey Code, Excess 3, SCII Code and its uses.	i, In cli 5 PI de qu tu	teractive assroom lecture, PT, emonstration, uiz,assignments, itorial	Teacher will explain the contents and provide handouts to students. Tea will conduct quiz/assignm tutorial to make students practice their knowledge.	acher nents	r ;/	07			-] { 	Text Bo Handou board, c Numeric Problen Workbo	oks, P ts, cha harts, cal ns ok	PT, lk
				S	CHEME OF ASSESSMENT	•								
S. No.	Metho	d of Assessment		Description o	of Assessment	N	Maxi Ma	mum Irks		Resources Required			Externa / Interna	
LO-02	LO-02 End Semester Theory 1. Li Exam 2. P			t will be asked to t out different coo form given binar ferent techniques	o(and/or): des and example of each y operation using 5.		1	0	Qı	Question paper, Rating scale			ale Externa	
			A	DITIONAL INSTR	UCTIONS FOR THE HOD	'FAC	CULT	Y (IF AN	1Y)					
						1								

					DUTCOME							Code Code		
							C 0		2	0		2	3	
COURS	E NAME	Digital Techniqu	е											
CO Des	cription	Design simple Logic	Circuit	with logic gates by a	pplying Boolean laws and rule	s on (expression							
LO Des	cription	Draw symbol and	write tru	th table & logical	expression for allthe gates.									
		·			SCHEME OF STUDY									
S. No.	L	earning Content		Teaching – Learning Method	Description of T-L Proce	SS	Teach Hrs.	/1	Pract Fut H	t. rs.	LRs Required			Remarks
LO-03	LO-03 Logic Gates: Basic concepts of Diode/transistor switch circuit, I Gates Symbols, Truth Table and Logical expression of Basic logic gates-AND, OR, NOT Universal Gates-NAND and NOR Special Purpose Gates-EX-OR, EX-NOR Realization of All Other Gates Us Universal Gates		Logic d c Jsing	Interactive classroom lecture, PPT, demonstration, quiz,assignment s, tutorial	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.		07				Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.			
					SCHEME OF ASSESSMEN	IT								
S. No.	Metho	d of Assessment		Description	of Assessment	M m	aximu Marks	Resources Required					External / Internal	
LO-03	End S	Semester Theory Exam	Stude 1. Dr ga 2. Re	ent will be asked raw symbol and tru tes. ealize the given ga	l to (and/or): uth table of given logic tes using universal gates.		10	Question paper, Rating scale			cale	External		
				ADDITIONAL INS	TRUCTIONS FOR THE HOL)/ F/	ACULTY (IF AN	IY)					

				SCHEME FO	DR LEARNING	Branch Co	ode (Course Code	e CO Cod	LO Code	
KGPV		oma wing) B	nopai	OUT	COME	C 0	2	0	2	4	Format No. 4
COURS	E NAME	Digital Techniqu	ie								-
CO Des	cription	Design simple Logi	c Circuit wit	h logic gates by applyir	ng Boolean laws and rules	on expressio	n.				
LO Des	cription	Solve equation us	ing Boolea	n algebra and K-map							
					SCHEME OF STUDY						
S. No.		Learning Conten	t	Teaching – Learning Method	Description of T-L Process	Teac h Hrs.	Pract. /Tut Hrs	•	LRs Req	uired	Remarks
LO-04	D-04 Boolean Algebra-Rules and Laws of Boolean Algebra, De-Morgan's Theorem Duality Theorem Introduction to logic design with Karnaugh map Simplification of Boolean Function up-to 4 variables (2,3,4 variable), Don't Care Condition Boolean Representation-Sum of Product and product of Sum , Min Term and Max		ws of Theorem. ith ition up-to n't Care of Product n and Max	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain t contents and provide handouts to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.	he 08	08 Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.				
	1			SCH	IEME OF ASSESSMEN	Т					I
S. No.	Metho	d of Assessment		Description of As	sessment	Maximu m Marks	Res	ources	Require	d	External / Internal
LO-04	End S	Semester Theory Exam	Student 1. State 2. Simpl 3. Expre	t will be asked to (a De-Morgan's theorem ify the Boolean functio ess the Boolean functio	nd/or): & Duality theorem in using K-map n as PSO / SOP form.	10	Question paper + Rating scale.			scale.	External
			AD	DITIONAL INSTRUC	TIONS FOR THE HOD	/ FACULTY	(IF ANY)				

RGPV	/ (Diplo	ma Wing) B	hopal	SCH	EME FOR LEARNING	Branch	Code		Co	ourse Co	de	CO Code	LO Code	Forn	nat No 4
					OUTCOME	C 0			2	0		2	5		
COURS	E NAME	Digital Techniqu	е												
CO Des	cription	Design simple Logic	Circuit w	ith logic gate	s by applying Boolean laws and rules o	n express	ion.								
LO Des	cription	Implement and ver	rify truth	table of give	en logic gates and Boolean equation	•									
					SCHEME OF STUDY										
S. No.	Lear	ning Content	Tea Le M	iching – arning ethod	Description of T-L Process	Teac Hrs	:h	Prac Tut H	ct. / Hrs.		LRs	Req	uired		Remarks
LO-05	Verify tru OR, EX-OF NANDgate Implemen gate using gate and v Implemen table of D theorem. Implemen equation verifyout	th table of NOT and, R, EXNOR, NOR, es. at AND, OR and NOT g NOR and NAND verifytruth table. at and verify truth e-Morgan's at simple Boolean using gates and out	Lab demon PPT , ł practica assigni	stration, nands on e, lab ments.	 Teacher with support from lab staff will demonstrate the procedure of lab experiments. Student will conduct lab assignment based on these experiments. 			06	6	Lak Ha tra wit ins wit sof	o manua ndouts, iner ins th meas trumen th releva tware a ernet.	al, ch , expe suring uts, cc ant si and h	arts, erimer ents/k g omput imulat igh spo	ital iit er ion eed	
					SCHEME OF ASSESSMENT										
S. No.	Met	hod of Assessmen	t	De	scription of Assessment	Ma N	xim 1arl	num ks	ſ	Reso	urces R	Requi	ired	External / Internal	
LO-05	Pract	ical test in laborator	ry S 1. 2. 3	Student will Verify the Implemer . Verify De	be asked to truth table of given logic gate t logic gate using universal gate. -Morgan's theorem.		15	15 Rubrics, Rating scale]	Internal					

			ADDI		ONS FOR THE HOD,	/ FACULTY (IF ANY)				
				SCHEME FOR	LEARNING	Branch Coo	le	Course Code	CO Code	LO Code	Л
KGPV	סוקוט) י	ma w	ing) Bhopai	OUTCO	OME	C 0	2	2 0	3	6	Format No. 4
COURS	E NAME	Digital	Technique								
CO Des	cription	Learn th circuit.	ne minimization technic	ques to simplify the h	ardware requiremen	ts of digital o	ircuit and	d understa	nd the de	sign of (Combinational
LO Des	cription	Design	Adder, Subtractor. Enc	oder and Decoder circ	cuits						
				SCI	HEME OF STUDY						
			• • •	Teaching –			Теа	Pract.			
S. NO.		Learni	ng Content	Learning Method	Description of T	-L Process	ch Hrs.	/ Tut Hrs.	LRS Re	equired	Remarks
LO-06	Half adder Half Subtra Basics of E Basics of D Decoder.	, Full add actor and ncoder, D Decoder, B	er Full Subtractor Decimal to BCD Encoder BCD -to -Seven Segments	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explai contents and provid to students. Teache conduct assignmen quiz/tutorial to mak practice their know	in the le handouts or will ts/ xe students vledge.	07		Text Boo Handouts board, ch Video leo NPTEL a	rs.	
				SCHEN	IE OF ASSESSMEN	Т		I			
S. No.	Metho Assess	od of ment		Description of Ass	essment		Maxim Mark	um s Re	sources	Require	ed External / Internal
LO-06	End Ser Theory	mester Exam	Student will be ask 1. What is an enc 2. Give the logic e 3. Design a full ac 4. Design a 2:4 de	ed to (and/or): oder? expression for sum and lder using two half add ecoder using basic gates	carry in full adder circu ers and an OR gate. 5.	uit.	10	Question paper , Rating scale		ng External	

				ADDITIONAL IN	STRUCTIONS FOR THE HOD	/ FACULTY	(IF ANY)				
				SCHEN	1E FOR LEARNING	Branch C	ode (Course Code	CO Code	LO Code	
KGPV	י (טוסוט)	ma v	ving) Bhopa	al	OUTCOME	C 0	2	0	3	7	Format No. 4
COURS	E NAME	Digita	l Technique			<u> </u>	! !	<u> </u>		-	,
CO Des	cription	Learn t	he minimization teo	chniques to simplify	the hardware requirements of d	igital circuit	and understa	ind the desig	n of Co	mbinat	ional circuit.
LO Des	cription	Explai	n differenttypes of	multiplexers, de-	multiplexers and code converto	r.					
		<u>.</u>			SCHEME OF STUDY						
S. No.	Le	earning	Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs	LRs	Requi	red	Remarks
LO-07	Multiplexe Applicatio Demultipl Demultipl Code Con (74184), E	er/Demu ons of Mu exer, 4:1 exer vertor-Bo binary to	Iltiplexer- Iltiplexer and Multiplexer, 1:4 CD to Binary BCD (74185A)	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.	07		Text Bo Handou board, c lecture- others.	oks, PI ts, chal harts, \ NPTEI	PT, k ∕ideo ₋ and	
					SCHEME OF ASSESSMEN	Г					
S. No.	Metho Assess	od of ment		Descriptio	on of Assessment		Maxim um Marks	Resource	es Req	uired	External / Internal

LO-07	Mid Ser Theory	nester Exam	Student will be 1. Design and im 2. Explain given	e asked to (and/or): plement the conversion o Multiplexer/Demultiplex	circuits for BCD to binary. er and list out application c	of it		10	Questic Ratin	on pape ng scale	er,	Internal
			1	ADDITIONAL INSTRU	JCTIONS FOR THE HOD	/ FACUL	TY (I	F ANY)				
						Bran	:h Code	Co	urse Code	со	LO	
RGPV	' (Diplo	oma V	Ving) Bhopa					2		Code	Code	Format No. 4
001100	COURSE NAME Digital Technique OUTCOME C 0 2 0 3 8											
COURS		Digita	i iecnnique									
CO Des	cription	Learn t	he minimization teo	chniques to simplify the h	ardware requirements of c	ligital circu	iit and	d understan	d the desig	n of Co	mbinatio	onal circuit.
LO Deso	cription	Implen	nent and verify giv	ven combinational logic	e circuits.							
		1			SCHEME OF STUDY							
S. No.	L	earning	Content	Teaching – Learning Method	Description of T-L Process	Tea Hr	ch s.	Pract. / Tut Hrs.	LR	s Requ	uired	Remarks
LO-08 Implement and verify truth table of Half & Full adder, Half & Full Subtractor. Verify truth table of 4:1 Multiplexer, 1:4 De-multiplexer Design and implement Decoder(2:4) and Encoder(4:2) Study of Code converter and BCD adder.					06	Lab man Handout trainer ir with mea instrume with rele software internet.	ual, ch cs, expe nstrum asuring ents, co evant s e and h	arts, eriment ents /k g ompute imulatio igh spe	al it r on ed			
				SC	CHEME OF ASSESSMEN	T						
S. No.	Met	hod of <i>l</i>	Assessment	Description of	of Assessment	Maxim m Mark	u s	Resources Required			External / Internal	

LO-09	Pract	ical test in laboratory	St 1. 2.	t udent will be Verify the giver Verify the giver & encoder.	asked to n Adder/Subtractor circuit. n Multiplexer/De-multiplexer.	20		Rubr	rics, R	ating	scale		External
	1		AD	DITIONAL INS	STRUCTIONS FOR THE HOD,	/ FACULTY	(IF AN	Y)					1
				SCHEM	IE FOR LEARNING	Branch (Code	Co	urse Cod	e	CO Code	LO Code	
KGPV		oma wing) Bh	opai		Ουτςομε	C 0		2	0		4	9	Format No. 4
COURS	E NAME	Digital Technique				· ·	<u> </u>						·
CO Des	cription	Obtain basic knowled	ge of log	gic families for im	plement logics within integrated	l circuit.							
LO Des	cription	Define digital integra	ed circu	its.									
		·			SCHEME OF STUDY								
S. No.	L	earning Content		Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pra /Tut	ict. Hrs.		LRs I	Requi	red	Remarks
LO-9Introduction to Digital Integrated CircuitsInteractive classroomTeacher will explain the contents and provide07Characteristics of Digital IC'slecture, PPT, lecture, PPT, demonstration, quiz, assignments.Teacher will conduct07				-	Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.								
					SCHEME OF ASSESSMEN	Г							
S. No.	S. No. Method of Assessment			Descriptio	on of Assessment	Maxim	um Ma	rks	Reso	urce	s Requ	uired	External / Internal

LO-9	LO-9 Mid Semester Theory Exam 2. D		Studen 1. Expl 2. Draw	t will be aske ain the digital i v the Character	d to (and/or): ntegrated circuits. istics of Digital IC's.	10 Question pap Rating scale		on pap g scale	er,	Inter	nal			
			AD		STRUCTIONS FOR THE HOD/	FACU	LTY (IF	ANY)						
RGPV	/ (Diplo	oma Wing) B	hopal	SCHEN	IE FOR LEARNING	Bra	nch Code	c	ourse C	ode	CO Code	LO Code	Form	nat No. 4
					OUTCOME	С	0	2	0		4	10	TOTT	
COURS	E NAME	Digital Techniqu	e											
CO Des	cription	Obtain basic knowle	edge of log	ic families for in	plement logics within integrated	circuit.								
LO Des	cription	Compare the chara	cteristics	of different log	ic families.									
					SCHEME OF STUDY									
S. No.	L	earning Content		Teaching – Learning Method	Description of T-L Proces	is 1	「each Hrs.	Prac /Tut H	t. Irs.	l	.Rs Re	quired		Remarks
LO-10	Character Power Dia Fan Out, logic Fam MOS Analysis o state Log	ristics of Logic Familie ssipation, Speed, Fan Propagation delay Tim ilies –RTL, DTL, IIL, EC of open collector and t	s – In in cla ne leo L, Vi de tri – qu as	teractive assroom cture, PPT, ideo, emonstration, tiz, signments.	Teacher will explain the contents and provide handour to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.	ts s	08			Text Hand charts NPTE	Books, outs, cl s, Video EL and	PPT, halk bo b lectur others.	ard, e-	
					SCHEME OF ASSESSMENT	•								
S. No.	No. Method of Assessment			Descriptio	on of Assessment	M	aximur	n Marks	5	Resou	urces F	Requir	ed	External / Internal

LO-10	LO-10 End Semester Theory Exam 2. Dra logi			will be asked are logic famili circuit and exp	to (and/or): les on given parameters. lain open collector and tri state		Questi	Question paper , Ratir scale.			External	
			AD	DITIONAL IN	STRUCTIONS FOR THE HOD	/ FACULTY	(IF ANY)					
				SCHEN	IE FOR LEARNING	Branch C	ode (Course Code	CO Code	LO Code		
KGPV	סוקוט) י	ima wing) E	snopai		Ουτςομε	C 0	C 0 2		5	11	Form	at No. 4
COURS	E NAME	Digital Techniq	ue									
CO Des	cription	Understand the de	esign of Sequ	uential Circuits s	uch as Flip Flop, Registers and Co	ounters.						
LO Deso	ription	Draw circuit ofdi	fferent flip-	-flopsand expla	in itsoperation.							
		1			SCHEME OF STUDY							
S. No.	Le	earning Content		Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs	. LRs	Requi	red	R	emarks
LO-11	LO-11 One-bit Memory Cell, Concept of Intera clock Signal classr Flip Flop –S-R, Clocked R-S, JK, JK lectur Master Slave, T and D Flip Flop, Video Application of Flip Flop demo quiz, assign			teractive assroom cture, PPT, ideo, emonstration, iiz, signments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.	06		Text Bo Handout board, cl lecture- others.	Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.			
					SCHEME OF ASSESSMEN	Г						
S. No.	No. Method of Assessment			Descriptio	n of Assessment	Maxim	um Marks	Resources Required			Ext In	ternal / iternal

LO-11	End Se	emester Theory Exam	Studen 1. Expla 2. Real 3. Drav	It will be asked ain the working M ize JK Flip Flop usin v the state table an	to (and/or): aster/Slave JK FF ng SR Flip Flop nd excitation table of T flip flop.		10	Questio Ratin	Question paper, Rating scale.		External
			ļ	ADDITIONAL IN	STRUCTIONS FOR THE HOD	/ FACULTY	(IF ANY)				
RGPV	(Dinlo	ma Wing) F	Shona	SCHEN	IE FOR LEARNING	Branch C	ode (Course Code	CO Code	LO Code	
			пора		OUTCOME	C 0	2	0	5	12	Format No. 🛥
COURS	COURSE NAME Digital Te		ue								
COurse Market Digital recinique Course Market Digital recinique											
LO Deso	cription	Define CMOS, M	IESFET :	and UJT.							
		·			SCHEME OF STUDY						
S. No.	Le	earning Content		Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs	LRs	Requi	red	Remarks
LO-12	Registers, Shift Register, types of Shift Register-SISO, SIPO, PISO, PIPO Counters-Basics of counter and its applicationsInteractive contents and provide handouts to students.06Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.Register-SISO, SIPO, PISO, PIPO Counters-Basics of counter and its applicationsInteractive classroom lecture, PPT, Video, demonstration, quiz, assignments.Teacher will explain the contents and provide to studentsText Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.										
	SCHEME OF ASSESSMENT										
S. No.	. No. Method of Assessment			Descriptic	on of Assessment	Maxim	um Marks	Resour	ces Re	equire	d External / Internal

LO-12	Mid S	emester Theory Exam 2	 dent will be asked Design and explain Up/Down ripple co Draw a 4-bit SISO S register and draw 	d to (and/or): In the working of an 4-bit Dunter SIPO, PIPO and PISO shift its waveforms		10	Question pape scale.		r , Ratii	ng External
			ADDITIONAL INS	STRUCTIONS FOR THE HOD	/ FACULTY	(IF ANY)				
	(Dinla	ma Wing \ Phon	SCHEM	E FOR LEARNING	Branch C	ode Co	ourse Code	CO Code	LO Code	Λ
				OUTCOME	C 0	2	0	5	13	Format No. 🕂
COURS	E NAME	Digital Technique								
CO Des	cription	Understand the design of	Sequential Circuits s	uch as Flip Flop, Registers and Co	ounters.					
LO Des	cription	Design and Implement gi	ven SequentialLogic C	Circuits and verify it						
		·		SCHEME OF STUDY						
S. No.	L	earning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs	Requi	red	Remarks
LO-13	Verify tru flip-flop. Design an registers o Design an counter u Design an counter u	th table of RS, JK, D and T Id Implement Shift using D flip-flop Id Implement ripple sing J-K flip-flop Id Implement synchronous sing J-K flip-flops.	Lab demonstration, PPT , hands on practice, labassignments.	 Teacher with support from lab staff will demonstrate the procedure of lab experiments. Student will conduct lab assignment based on these experiments. 		08	Lab manual, charts, Handouts, experimental trainer instruments/kit with measuring instruments, computer with relevant simulation software and high speed internet.			
				SCHEME OF ASSESSMEN	Т					

S. No.	Method of Assessment	Description of Assessment	Maximu m Marks	Resources Required	External / Internal
LO-13	Practical test in laboratory	Student will be asked to1. Verify the given flip flop.2. Design given counter using flip flop.	15	Rubrics, Rating scale	Internal
		ADDITIONAL INSTRUCTIONS FOR THE HO	D/ FACULTY	(IF ANY)	

Rajiv Gandhi Proudyogiki Vishwavidyalaya Office Complex, A-4 Gautam Nagar, Bhopal (M. P.) INTERNAL ASSESSMENT (PRACTICAL COMPONENT) MARKS

Exam	ination Centre										
Bran	ch	CSE,IT,CHM									
Term	/ Semester	II semester		Name o	f Examina	ation	April 2021				
Cours	se Code	203/7151		Course Na	lame DIGITAL TECHNIQUES(PRACTICAL COMPONENT)				CTICAL		
	Marks Obtained										
			CC) No.	2	5					
			LO	No.	5	13					
			Max.	Marks	15	15					
S. No.	Enrollment No	p. 9	tudent Name	e							
1	1										
2											
NOTE prop	NOTE: Max. Marks for Internal Assessment Practical Component is 30. Marks obtained by the students will be proportionately reduced to 20 , while processing the result.										

		R Office INTERN	ajiv Gandhi e Complex, AL ASSESSN	Proudyog A-4 Gauta 1ENT (THEC	iki Vishwa m Nagar, DRY COM	avidya Bhopa PONE	alaya al (M. P.) NT) MARKS								
Examination	Centre														
Branch		CSE,IT,CHM													
Term / Seme	ster	II semester		Name of	Examinat	ion	April 2021								
Course Code	Course Code 203/7151 Course Name DIGITAL TECHNIQUES(THEORY COMPONENT)														
					Marks Obtained										
			CO I	No.	1	3	4								
			LOI	No.	1	7	9								
			Max. N	Marks	10	10	10								
S. No. Enroll	ment No	o. Stud	dent Name												
1															
2															
NOTE: Max. N	Aarks fo	r Internal Assessm	TE: Max. Marks for Internal Assessment Theory Component is 30.												

NOTE: End Sem Practical Examination should be conducted for a Max Marks of 30