RGPV (DIPLOMA WING) BHOPAL	OBE CURRICULUM FOR THE COURSE	FORMAT-3	Sheet No. 1/5
Branch	**Computer Science and Engineering**	**Semester**	**II**

Course Code		**Course Name**	**Digital Technique**	

Course Outcome 1	Perform conversion among different number systems, and became familiar with basic codes used in digital computer.	Teach Hrs.	Marks
Learning Outcome 1	Define signals and convert onenumber systemsto another.**(Cognitive)**	07	10
Contents	Definition of Signal,Comparisons Between Analog and Digital signal. Advantages and disadvantages of Digital Circuits. Number System-Introduction to binary, octal, decimal and hexadecimal number systems Conversion between number system.		
Method of Assessment	Internal		
Learning Outcome 2	Explain differentcodes andperform binary arithmetic.**(Cognitive)**	07	10
Contents	Binary Arithmetic-Binary addition, subtraction, Multiplication and division. 1's and 2's complements and its utilization Codes-BCD, Grey Code, Excess 3, EBCDIC, ASCII Code and its uses..		
Method of Assessment	External		

Branch	Computer Science and Engineering		Semester	II

Course Code		Course Name	Digital Technique	

Course Outcome 2	Design simple Logic Circuit with logic gates by applying Boolean laws and rules on expression.	Teach Hrs.	Marks
Learning Outcome 3	Draw symbol andwrite truth table & logical expression for allthe gates.(Cognitive)	07	10
Contents	Logic Gates: Basic concepts of Diode/transistor switch circuit, Logic Gates Symbols, Truth Table and Logical expression of Basic logic gates-AND,OR,NOT Universal Gates-NAND and NOR Special Purpose Gates-EX-OR,EX-NOR Realization of All Other Gates Using Universal Gates		
Method of Assessment	External		
Learning Outcome 4	Solve equation using Boolean algebra and K-map.(Cognitive)	08	10
Contents	Boolean Algebra-Rules and Laws of Boolean Algebra, De-Morgan's Theorem. Duality Theorem Introduction to logic design with Karnaugh map Simplification of Boolean Function up-to 4 variables(2,3,4 variable), Don't Care Condition Boolean Representation-Sum of Product and product of Sum, Min Term and Max term		
Method of Assessment	External		
Learning Outcome 5	Implement and verify truth table of given logic gates and Boolean equation. (Psychomotor)	06	15
Contents	Verify truth table of NOT and, OR, EX-OR, EXNOR, NOR, NANDgates. Implement AND, OR and NOT gate using NOR and NAND gate and verifytruth table. Implement and verify truth table of De-Morgan's theorem. Implement simple Boolean equation using gates and verifyoutput.		
Method of Assessment	Internal		

RGPV (DIPLOMA WING) BHOPAL	OBE CURRICULUM FOR THE COURSE	FORMAT-3	Sheet No. 3/5
Branch	**Computer Science and Engineering**	**Semester**	**II**
Course Code		**Course Name**	**Digital Technique**

Course Outcome 3	Learn the minimization techniques to simplify the hardware requirements of digital circuit and understand the design of Combinational circuit.	Teach Hrs.	Marks
Learning Outcome 6	Design Adder, Subtractor. Encoder and Decoder circuits.**(Cognitive)**	07	10
Contents	Half adder, Full adder Half Subtractor and Full Subtractor Basics of Encoder,Decimal to BCD Encoder Basics of Decoder,BCD -to -Seven Segments Decoder.		
Method of Assessment	External		
Learning Outcome 7	Explain differenttypes of multiplexers, demultiplexers and code convertor.**(Cognitive)**	07	10
Contents	Multiplexer/Demultiplexer-Applications of Multiplexer and Demultiplexer,4:1 Multiplexer,1:4 Demultiplexer Code Convertor-BCD to Binary (74184),Binary to BCD(74185A)		
Method of Assessment	Internal		
Learning Outcome 8	Implement and verify given combinational logic circuits. **(Psychomotor)**	06	20
Contents	Implement and verify truth table of Half & Full adder, Half & Full Subtractor Verify truth table of 4:1 Multiplexer, 1:4 De-multiplexer Design and implement Decoder(2:4) and Encoder(4:2) Study of Code converter and BCD adder.		
Method of Assessment	External		

Branch	Computer Science and Engineering		Semester	II

Course Code		Course Name	Digital Technique	

Course Outcome 4	Obtain basic knowledge of logic families for implement logics within integrated circuit.	Teach Hrs	Marks
Learning Outcome 9	Define digital integrated circuits. **(Cognitive)**	07	10
Contents	Introduction to Digital Integrated Circuits Characteristics of Digital IC's		
Method of Assessment	Internal		
Learning Outcome 10	Compare the characteristics of different logic families.**(Cognitive)**	08	10
Contents	Characteristics of Logic Families –Power Dissipation, Speed, Fan in Fan Out, Propagation delay Time logic Families –RTL, DTL, IIL, ECL, MOS Analysis of open collector and tri –state Logic		
Method of Assessment	External		

RGPV (DIPLOMA WING) BHOPAL	OBE CURRICULUM FOR THE COURSE	FORMAT- 3	Sheet No. 5/5

Branch	Computer Science and Engineering		Semester		II

Course Code			Course Name	Digital Technique	

Course Outcome 5	Understand the design of Sequential Circuits such as Flip Flop, Registers and Counters.	Teach Hrs	Marks
Learning Outcome 11	Draw circuit ofdifferent flip-flopsand explain itsoperation.**(Cognitive)**	06	10
Contents	One-bit Memory Cell, Concept of clock Signal Flip Flop –S-R, Clocked R-S, JK, JK Master Slave, T and D Flip Flop, Application of Flip Flop		
Method of Assessment	External		
Learning Outcome 12	Explaindifferent types ofshift register and counter. **(Cognitive)**	06	10
Contents	Registers, Shift Register, types of Shift Register-SISO, SIPO, PISO, PIPO Counters-Basics of counter and its applications		
Method of Assessment	External		
Learning Outcome 13	Design and Implement given SequentialLogic Circuits and verify it.**(Psychomotor)**	08	15
Contents	Verify truth table of RS, JK, D and T flip-flop. Design and Implement Shift registers using D flip-flop Design and Implement ripple counter using J-K flip-flop Design and Implement synchronous counter using J-K flip-flops.		
Method of Assessment	Internal		

SuggestedListofExperiments:

S.No	Experiment list
1.	Study and Verify the truth table of logic gates (74xx series).
2.	Realization of AND, OR, NOT and Ex-OR logic gates using NAND and NOR gate
3.	Verification of De-Morgan's theorem
4.	Implement simple Boolean equation using gates and verifyoutput.
5.	Implement and verify truth table of Half and Full adder.
6.	Implement and Verify truth table of Half and Full Subtractor
7.	Study and Verify truth table of 4:1 Multiplexer
8.	Study and Verify truth table of 1:4 De-Multiplexer
9.	Design and implement 2:4 Decoder.
10.	Design and implement 4:2 Encoder.
11.	Study of gray to binary code convertor using gates
12.	Study of BCD adder
13.	Verification of truth table of RS, JK, D and Tflip flop using IC's.
14.	Design and ImplementShift registers using D flip-flop
15.	Design and Implement ripple counter using J-K flip-flop
16.	Design and Implement synchronous counter using J-K flip-flops.

ReferenceBooks/WebPortals:

1.		
2.		
3.		
4.		
5.		
6.		
7.		

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code		Course Code		CO Code	LO Code	Format No. 4
		C	0	2	0	1	1	

COURSE NAME	Digital Technique
CO Description	Perform conversion among different number systems, and became familiar with basic codes used in digital computer.
LO Description	Define signals and convert onenumber systemsto another

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-01	Definition of Signal, Comparisons Between Analog and Digital signal. Advantages and disadvantages of Digital Circuits. Number System-Introduction to binary, octal, decimal and hexadecimal number systems Conversion between number system.	Interactive classroom lecture, PPT, demonstration, quiz, assignments	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/ assignments/ tutorial.	07	--	Text Books, PPT, Handouts, chalk board, charts.Videos lectures- NPTEL& others	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-01	Mid Semester Theory Exam	**Student will be asked to**(and/or): 1. List out various advantages and disadvantages of digital circuits. 2. Compare analog and digital signal. 3. Define number system and give example of each 4. Simple numerical on conversion of number system.	10	Question paper, Rating scale	Internal

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

COURSE NAME	Digital Technique
CO Description	Perform conversion among different number systems, and became familiar with basic codes used in digital computer.
LO Description	Explain differentcodes and perform binaryarithmetic..

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-02	Binary Arithmetic-Binary addition, subtraction, Multiplication and division. 1's and 2's complements and its utilization Codes-BCD, Grey Code, Excess 3, EBCDIC, ASCII Code and its uses..	Interactive classroom lecture, PPT, demonstration, quiz,assignments, tutorial	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/assignments/ tutorial to make students practice their knowledge.	07	--	Text Books, PPT, Handouts, chalk board, charts, Numerical Problems Workbook	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-02	End Semester Theory Exam	**Student will be asked to**(and/or): 1. List out different codes and example of each 2. Perform given binary operation using different techniques.	10	Question paper, Rating scale	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

		OUTCOME						Code	Code	
								C 0	2 0	2 3

COURSE NAME	Digital Technique
CO Description	Design simple Logic Circuit with logic gates by applying Boolean laws and rules on expression.
LO Description	Draw symbol andwrite truth table & logical expression for allthe gates.

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-03	Logic Gates: Basic concepts of Diode/transistor switch circuit, Logic Gates Symbols, Truth Table and Logical expression of Basic logic gates-AND, OR, NOT Universal Gates-NAND and NOR Special Purpose Gates-EX-OR, EX-NOR Realization of All Other Gates Using Universal Gates	Interactive classroom lecture, PPT, demonstration, quiz,assignments, tutorial	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.	07	--	Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-03	End Semester Theory Exam	**Student will be asked to**(and/or): 1. Draw symbol and truth table of given logic gates. 2. Realize the given gates using universal gates.	10	Question paper, Rating scale	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

COURSE NAME	Digital Technique
CO Description	Design simple Logic Circuit with logic gates by applying Boolean laws and rules on expression.
LO Description	Solve equation using Boolean algebra and K-map

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-04	Boolean Algebra-Rules and Laws of Boolean Algebra, De-Morgan's Theorem. Duality Theorem Introduction to logic design with Karnaugh map Simplification of Boolean Function up-to 4 variables (2,3,4 variable), Don't Care Condition Boolean Representation-Sum of Product and product of Sum , Min Term and Max term	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.	08	--	Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-04	End Semester Theory Exam	**Student will be asked to**(and/or): 1. State De-Morgan's theorem & Duality theorem 2. Simplify the Boolean function using K-map.. 3. Express the Boolean function as PSO / SOP form.	10	Question paper + Rating scale.	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code		Course Code		CO Code	LO Code	Format No. **4**
		C	0	2	0	2	5	

COURSE NAME	Digital Technique
CO Description	Design simple Logic Circuit with logic gates by applying Boolean laws and rules on expression.
LO Description	Implement and verify truth table of given logic gates and Boolean equation.

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. / Tut Hrs.	LRs Required	Remarks
LO-05	Verify truth table of NOT and, OR, EX-OR, EXNOR, NOR, NANDgates. Implement AND, OR and NOT gate using NOR and NAND gate and verifytruth table. Implement and verify truth table of De-Morgan's theorem. Implement simple Boolean equation using gates and verifyoutput	Lab demonstration, PPT , hands on practice, lab assignments.	• Teacher with support from lab staff will demonstrate the procedure of lab experiments. • Student will conduct lab assignment based on these experiments.		06	Lab manual, charts, Handouts, experimental trainer instruments/kit with measuring instruments, computer with relevant simulation software and high speed internet.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-05	Practical test in laboratory	**Student will be asked to** 1. Verify the truth table of given logic gate 2. Implement logic gate using universal gate. 3. Verify De-Morgan's theorem.	15	Rubrics, Rating scale	Internal

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code		Course Code		CO Code	LO Code	Format No. 4
		C	0	2	0	3	6	

COURSE NAME	Digital Technique
CO Description	Learn the minimization techniques to simplify the hardware requirements of digital circuit and understand the design of Combinational circuit.
LO Description	Design Adder, Subtractor. Encoder and Decoder circuits

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. / Tut Hrs.	LRs Required	Remarks
LO-06	Half adder, Full adder Half Subtractor and Full Subtractor Basics of Encoder, Decimal to BCD Encoder Basics of Decoder, BCD -to -Seven Segments Decoder.	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.	07	--	Text Books, PPT, Handouts, chalk board, charts, Video lecture-NPTEL and others.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-06	End Semester Theory Exam	**Student will be asked to**(and/or): 1. What is an encoder? 2. Give the logic expression for sum and carry in full adder circuit. 3. Design a full adder using two half adders and an OR gate. 4. Design a 2:4 decoder using basic gates.	10	Question paper , Rating scale	External

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	Branch Code		Course Code		CO Code	LO Code	Format No. **4**
		C	0	2	0	3	7	

COURSE NAME	**Digital Technique**
CO Description	Learn the minimization techniques to simplify the hardware requirements of digital circuit and understand the design of Combinational circuit.
LO Description	Explain differenttypes of multiplexers, de-multiplexers and code convertor.

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-07	Multiplexer/Demultiplexer-Applications of Multiplexer and Demultiplexer, 4:1 Multiplexer, 1:4 Demultiplexer Code Convertor-BCD to Binary (74184), Binary to BCD (74185A)	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.	07	--	Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal

LO-07	Mid Semester Theory Exam	**Student will be asked to** (and/or): 1. Design and implement the conversion circuits for BCD to binary. 2. Explain given Multiplexer/Demultiplexer and list out application of it	10	Question paper , Rating scale	Internal

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	Branch Code		Course Code		CO Code	LO Code	Format No. **4**
		C	*0*	*2*	*0*	*3*	*8*	

COURSE NAME	**Digital Technique**
CO Description	Learn the minimization techniques to simplify the hardware requirements of digital circuit and understand the design of Combinational circuit.
LO Description	Implement and verify given combinational logic circuits.

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. / Tut Hrs.	LRs Required	Remarks
LO-08	Implement and verify truth table of Half & Full adder, Half & Full Subtractor. Verify truth table of 4:1 Multiplexer, 1:4 De-multiplexer Design and implement Decoder(2:4) and Encoder(4:2) Study of Code converter and BCD adder.	Lab demonstration, PPT , hands on practice, lab assignments.	• Teacher with support from lab staff will demonstrate the procedure of lab experiments. • Student will conduct lab assignment based on these experiments.		06	Lab manual, charts, Handouts, experimental trainer instruments /kit with measuring instruments, computer with relevant simulation software and high speed internet.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal

LO-09	Practical test in laboratory	**Student will be asked to** 1. Verify the given Adder/Subtractor circuit. 2. Verify the given Multiplexer/De-multiplexer. & encoder.	20	Rubrics, Rating scale	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	**Branch Code**		**Course Code**		**CO Code**	**LO Code**	Format No. **4**
		C	0	2	0	4	9	

COURSE NAME	**Digital Technique**
CO Description	Obtain basic knowledge of logic families for implement logics within integrated circuit.
LO Description	Define digital integrated circuits.

SCHEME OF STUDY

S. No.	**Learning Content**	**Teaching – Learning Method**	**Description of T-L Process**	**Teach Hrs.**	**Pract. /Tut Hrs.**	**LRs Required**	**Remarks**
LO-9	Introduction to Digital Integrated Circuits Characteristics of Digital IC's	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz / tutorial to make students practice their knowledge.	07	--	Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.	

SCHEME OF ASSESSMENT

S. No.	**Method of Assessment**	**Description of Assessment**	**Maximum Marks**	**Resources Required**	**External / Internal**

LO-9	Mid Semester Theory Exam	**Student will be asked to** (and/or): 1. Explain the digital integrated circuits. 2. Draw the Characteristics of Digital IC's.	10	Question paper, Rating scale.	Internal

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	**Branch Code**		**Course Code**		**CO Code**	**LO Code**	Format No. **4**
		C	0	2	0	4	10	

COURSE NAME	**Digital Technique**
CO Description	Obtain basic knowledge of logic families for implement logics within integrated circuit.
LO Description	Compare the characteristics of different logic families.

SCHEME OF STUDY	

S. No.	**Learning Content**	**Teaching – Learning Method**	**Description of T-L Process**	**Teach Hrs.**	**Pract. /Tut Hrs.**	**LRs Required**	**Remarks**
LO-10	Characteristics of Logic Families – Power Dissipation, Speed, Fan in Fan Out, Propagation delay Time logic Families –RTL, DTL, IIL, ECL, MOS Analysis of open collector and tri – state Logic	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.	08	--	Text Books, PPT, Handouts, chalk board, charts, Video lecture-NPTEL and others.	

SCHEME OF ASSESSMENT	

S. No.	**Method of Assessment**	**Description of Assessment**	**Maximum Marks**	**Resources Required**	**External / Internal**

LO-10	End Semester Theory Exam	**Student will be asked to** (and/or): 1. Compare logic families on given parameters. 2. Draw circuit and explain open collector and tri state logic.	10	Question paper , Rating scale.	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	Branch Code		Course Code		CO Code	LO Code	Format No. **4**
		C	0	2	0	5	11	

COURSE NAME	**Digital Technique**
CO Description	Understand the design of Sequential Circuits such as Flip Flop, Registers and Counters.
LO Description	Draw circuit ofdifferent flip-flopsand explain itsoperation.

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-11	One-bit Memory Cell, Concept of clock Signal Flip Flop –S-R, Clocked R-S, JK, JK Master Slave, T and D Flip Flop, Application of Flip Flop	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/tutorial to make students practice their knowledge.	06	--	Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal

LO-11	End Semester Theory Exam	**Student will be asked to**(and/or): 1. Explain the working Master/Slave JK FF 2. Realize JK Flip Flop using SR Flip Flop 3. Draw the state table and excitation table of T flip flop.	10	Question paper , Rating scale.	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	**Branch Code**		**Course Code**		**CO Code**	**LO Code**	Format No. **4**
		C	*0*	*2*	*0*	*5*	*12*	

COURSE NAME	**Digital Technique**
CO Description	Understand the design of Sequential Circuits such as Flip Flop, Registers and Counters.
LO Description	Define CMOS, MESFET and UJT.

SCHEME OF STUDY

S. No.	**Learning Content**	**Teaching – Learning Method**	**Description of T-L Process**	**Teach Hrs.**	**Pract. /Tut Hrs.**	**LRs Required**	**Remarks**
LO-12	Registers, Shift Register, types of Shift Register-SISO, SIPO, PISO, PIPO Counters-Basics of counter and its applications	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments / quiz / tutorial to make students practice their knowledge.	06	--	Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.	

SCHEME OF ASSESSMENT

S. No.	**Method of Assessment**	**Description of Assessment**	**Maximum Marks**	**Resources Required**	**External / Internal**

| LO-12 | Mid Semester Theory Exam | **Student will be asked to** (and/or):
1. Design and explain the working of an 4-bit Up/Down ripple counter
2. Draw a 4-bit SISO SIPO, PIPO and PISO shift register and draw its waveforms | 10 | Question paper , Rating scale. | External |

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	Branch Code		Course Code		CO Code	LO Code	Format No. **4**
		C	0	2	0	5	13	

COURSE NAME	**Digital Technique**
CO Description	Understand the design of Sequential Circuits such as Flip Flop, Registers and Counters.
LO Description	Design and Implement given SequentialLogic Circuits and verify it

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-13	Verify truth table of RS, JK, D and T flip-flop. Design and Implement Shift registers using D flip-flop Design and Implement ripple counter using J-K flip-flop Design and Implement synchronous counter using J-K flip-flops.	Lab demonstration, PPT , hands on practice, labassignments.	• Teacher with support from lab staff will demonstrate the procedure of lab experiments. • Student will conduct lab assignment based on these experiments.	--	08	Lab manual, charts, Handouts, experimental trainer instruments/kit with measuring instruments, computer with relevant simulation software and high speed internet.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-13	Practical test in laboratory	**Student will be asked to** 1. Verify the given flip flop. 2. Design given counter using flip flop.	15	Rubrics, Rating scale	Internal
ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)					

Rajiv Gandhi Proudyogiki Vishwavidyalaya
Office Complex, A-4 Gautam Nagar, Bhopal (M. P.)
INTERNAL ASSESSMENT (PRACTICAL COMPONENT) MARKS

Examination Centre								
Branch	CSE,IT,CHM							
Term / Semester	II semester		Name of Examination		April 2021			
Course Code	203/7151		Course Name		DIGITAL TECHNIQUES**(PRACTICAL COMPONENT)**			
					Marks Obtained			
			CO No.	2	5			
			LO No.	5	13			
			Max. Marks	15	15			
S. No.	**Enrollment No.**		**Student Name**					
1								
2								
NOTE: Max. Marks for Internal Assessment Practical Component is 30. Marks obtained by the students will be proportionately reduced to 20 , while processing the result.								

Rajiv Gandhi Proudyogiki Vishwavidyalaya
Office Complex, A-4 Gautam Nagar, Bhopal (M. P.)
INTERNAL ASSESSMENT (THEORY COMPONENT) MARKS

Examination Centre								
Branch	CSE,IT,CHM							
Term / Semester	II semester		Name of Examination		April 2021			
Course Code	203/7151		Course Name		DIGITAL TECHNIQUES**(THEORY COMPONENT)**			
					Marks Obtained			
			CO No.	1	3	4		
			LO No.	1	7	9		
			Max. Marks	10	10	10		
S. No.	**Enrollment No.**		**Student Name**					
1								
2								
NOTE: Max. Marks for Internal Assessment Theory Component is 30.								

NOTE: End Sem Practical Examination should be conducted for a Max Marks of 30