RGPV (DIPLOMA WING) BHOPAL	OBE CURRICULUM FOR THE COURSE	FORMAT-3	Sheet No. 1/5

Branch	Electronics & Tele-communication	Semester	3
Course Code		Course Name	Digital Electronics

Course Outcome 1	Examine the structure of various number system, codes and logic gates.	Teach Hrs	Marks
Learning Outcome 1	List out different types of number system & code and convert one to another. *(Cognitive)*	8	10
Contents	**Number System:** Decimal number, binary number, octal and Hexadecimal number. **Binary Codes:** Weighted and un-weighted codes BCD, Gray, Excess-3. **Conversion of number system and code:** (Decimal number, binary number, octal and Hexadecimal number, BCD, Gray, Excess-3)		
Method of Assessment	External		
Learning Outcome 2	Perform various binary arithmetic operation. *(Cognitive)*	5	10
Contents	**Binary operations:** Binaryaddition,subtraction, Multiplication, Division. **Complement of number:** Complements:1's,2's,9'sand10's. Subtraction using 1's and2's complement.		
Method of Assessment	Internal		
Learning Outcome 3	Verify truth table of all the gates. *(Psychomotor)*	6	10
Contents	**Logic Gates:** Symbol, operation and truth-table: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR Realization of logic gates using universal gates. **Logic System:** Positive and negative logic system. Verification of the basic logic gates (AND, OR,NOT NAND , NOR ,EX-OR and EX-NOR).		
Method of Assessment	External		

RGPV (DIPLOMA WING) BHOPAL	OBE CURRICULUM FOR THE COURSE	FORMAT-3	Sheet No. 2/5

Branch	Electronics & Tele-communication	Semester	3
Course Code		Course Name	Digital Electronics

Course Outcome 2	Construct and Examine simple combinational digital circuit.	Teach Hrs	Marks
Learning Outcome 4	Verify Boolean algebra laws and theorems. *(Psychomotor)*	5	10
Contents	**Laws and theorems of Boolean algebra:** Boolean laws, De-Morgan's Theorem and Duality Theorem, Complement of Boolean equations. Verification of De- Morgan's theorem.		
Method of Assessment	Internal		
Learning Outcome 5	Solve Boolean expressions using K-map and realize its logic circuit. *(Cognitive)*	8	10
Contents	**Karnaugh-map:** Boolean expressions: Sum of product and product of sum, Karnaugh maps and its use forsimplification up to four variable Boolean expressions, Don't care condition. **Realization of logic equations:** The universal building blocks-NAND & NOR, AND-OR network, NAND-NAND Logic for implementation of Boolean expressions.		
Method of Assessment	External		
Learning Outcome 6	Implement different type of adder and subtractor circuits. *(Cognitive)*	5	10
Contents	**Adder and Subtractor Circuit:** Half adder, full adder, parallel binary adder, 8421 adder, half subtractor, full subtractor, parallel binary subtractor.		
Method of Assessment	External		
Learning Outcome 7	Design different type of coder and multiplexer circuits *(Psychomotor)*	8	10
Contents	**Coder Circuit:** Encoder, Decoder (2 to 4 line,3 to 8 line, BCD to Decimal, Decimal to7 segment) **MUX Circuit:** Multiplexers: 4 to1 and 8 to1. De-Multiplexers: 1 to 4 and 1 to 8.		

	(Block Diagram and Truth table) Verification of encoder, decoder, multiplexer and de-multiplexer circuit.
Method of Assessment	Internal

RGPV (DIPLOMA WING) BHOPAL	**OBE CURRICULUM FOR THE COURSE**	**FORMAT-3**	**Sheet No. 3/5**

Branch	**Electronics & Tele-communication**	**Semester**	**3**
Course Code		**Course Name**	**Digital Electronics**

Course Outcome 3	Analyze flip-flop circuit, counters, shift registers and understand their operation.	Teach Hrs.	Marks
Learning Outcome 8	Analyze the working of various flip-flops and verify its outputs. *(Psychomotor)*	8	10
Contents	**Flip-Flop:** S-R flip-flops(FF), D FF, Types of Triggering, Glitch, JK FF race around condition and remedies, JK Master Slave FF and T FF. Verification of various flip-flops		
Method of Assessment	Internal		
Learning Outcome 9	Draw and explain different type of registers. *(Cognitive)*	5	10
Contents	**Registers:** Shift Register (3 to 4 bits only)- introduction, circuitdiagram and waveforms of SISO, SIPO,PISO, PIPO shift registers.		
Method of Assessment	External		
Learning Outcome 10	Design different type of synchronous and asynchronous counters. *(Psychomotor)*	8	10
Contents	**Counters:** Asynchronous: Up/down counters, Up-down counters. Synchronous Counters. Up/down counters, Ring counter, Johnson counter. Design Mode-4 counters.		
Method of Assessment	External		

RGPV (DIPLOMA WING) BHOPAL	OBE CURRICULUM FOR THE COURSE	FORMAT-3	Sheet No. 4/5

Branch	Electronics & Tele-communication	Semester	3
Course Code		Course Name	Digital Electronics

Course Outcome 4	Demonstrate the functioning of A to D and D to A Converters.	Teach Hrs	Marks
Learning Outcome 11	Draw and explain various operation of D/A conversion circuits. *(Cognitive)*	5	10
Contents	**D/A Conversion**: Weighted resister, R-2R ladder network.		
Method of Assessment	Internal		
Learning Outcome 12	Draw and explain various operation of D/A conversion circuits. *(Cognitive)*	6	10
Contents	**A/D Conversion:** Counter type, Successive approximation, Flash type, Dual slope type.(Theoretical aspects)		
Method of Assessment	External		

RGPV (DIPLOMA WING) BHOPAL	OBE CURRICULUM FOR THE COURSE	FORMAT-3	Sheet No. 5/5

Branch	Electronics & Tele-communication	Semester	3
Course Code		Course Name	Digital Electronics

Course Outcome 5	Compare various digital logic family.	Teach Hrs.	Marks
Learning Outcome 13	Compare digital ICs on different parameters. *(Cognitive)*	6	10
Contents	**Characteristics of digital ICs:** Fan-in, Fan-out, Propagation delay, Power dissipation, Noise margins, Figure of merit. **Logic ICs:** NAND Gate using TTL, NOR gate using ECL.		
Method of Assessment	External		
Learning Outcome 14	Construct universal gates and inverter using MOS and CMOS logic. *(Cognitive)*	6	10
Contents	**Classifications of logic families:** Saturated and Non-saturated logic. **MOS and CMOS Logic:** MOS based NOT gate, Two input NAND & NOR gate. CMOS based NOT gate, Two input NAND & NOR gate.		
Method of Assessment	External		
Learning Outcome 15	Make use of PAL & PLA for implementation of Boolean expression and design simple logic circuit. *(Cognitive/Affective)*	6	10
Contents	**PLD:** PAL,PLA Implementation of Boolean expression using PAL,PLA (Up-to 2 variables)		
Method of Assessment	Internal		

Suggested Experiment:

S. No.	Practical Experiment	CO
1.	Verify the basic logic gates (AND, OR,NOT NAND , NOR ,EX-OR and EX-NOR).	CO302.2
2.	Verify De- Morgan's theorem.	CO302.2
3.	Verify half adder and full adder circuit using EX-OR, AND, OR logic gates.	CO302.2

4.	Verify half subtractor, full subtractor circuit using EX-OR, AND, OR logic gates.	CO302.2
5.	Verify parallel binary subtractor circuit.	CO302.2
6.	Verify 4 bit parallel adder circuit.	CO302.2
7.	Verify the 2 to 4 or 3 to 8 lines decoder circuit.	CO302.2
8.	Verify BCD to 7 segment decoder circuit.	CO302.2
9.	Verify the encoder circuit.	CO302.2
10.	Realize the minimized network of a given function and verify truth table.	CO302.2
11.	Verify the 4:1 or 8:1, multiplexer circuit.	CO302.2
12.	Verify the 1:4 or 1:8 de multiplexer circuit.	CO302.2
13.	Verify SR flip-flop and construct D flip-flop from it.	CO302.3
14.	Verify JK flip-flop and constructT flip-flop from it.	CO302.3
15.	Verify JK master slave flip-flop.	CO302.3
16.	Design Mode-4 Counters.	CO302.3
17.	Design and Develop mini project using digital logic.	CO302.2, CO302.3, CO302.4

Suggestions:

Experiments are expected to be performed

1. **Using breadboard/trainer kits.**
2. **Simulation software (anyone like: PSpice, TINA, Multisim, KiCAD, LTSpice, LabView, Simulink, Proteus, CircuitMaker etc.)**
3. **On virtual lab platforms available online (like: vlab.co.in, falstad.com/circuit etc.)**

SuggestedActivities:

1. **Interpret any one DataSheet of A to D or D to A Converter. (CO302.4)**
2. **List at least two IC's per Logic Family. (CO302.5)**

LEARNING RESOURCES:

Reference Books:

S. No.	Title of Book	Author	Publication
1.	Fundamentals of Digital Circuits	A. Anand Kumar	PHI, 2009 or latest
2.	Digital Electronics and Logic Design	Sharma Sanjay	S. K. Kataria& Sons, 2012 or latest
3.	Modern Digital Electronics	Jain R P	TMH, 2009 or latest
4.	Digital Electronics	K. Meena	PHI, 2009 or latest
5.	Digital Electronics Principles	Malvino& Leach	TMH, 2011 or latest
6.	Digital Electronics	Morris Mano	Pearson, 2008 or latest
7.	Digital Fundaments	Floyd Thomas L & Jain	Pearson, 2011 or latest
8.	Digital Electronics	Shiv Shankar Mishra	Satya Prakashan New Delhi

List of Software/Learning Websites:

1. www.nptel.iitm.ac.in
2. www.ocw.mit.edu
3. www.slideshare.net

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	0	3	3	0	3	1	1	

COURSE NAME	**Digital Electronics**
CO Description	Examine the structure of various number system, codes and logic gates.
LO Description	List out different types of number system & code and convert one to another.

SCHEME OF STUDY

S. No.	Learning Content	Teaching –Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-01	**Number System:** Decimal number, binary number, octal and Hexadecimal number. **Binary Codes:** Weighted and un-weighted codes BCD, Gray, Excess-3. **Conversion of number system and code:** (Decimal number, binary number, octal and Hexadecimal number, BCD, Gray, Excess-3)	Interactive classroom lecture, PPT, demonstration, quiz, assignments, tutorial	Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/ tutorial	5	3	Text Books, PPT, Handouts, chalk board, charts. Numerical Problems Workbook	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-01	End Semester Theory Exam	**Student will be asked to** (and/or) 1. Explain the given number system or binary code. 2. Convert given number system/ binary code to another.	10	Question paper, Rating scale	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	0	3	3	0	3	1	2	

COURSE NAME	**Digital Electronics**
CO Description	Examine the structure of various number system, codes and logic gates.
LO Description	Perform various binary arithmetic operation.

SCHEME OF STUDY

S. No.	Learning Content	Teaching –Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-02	**Binary operations:** Binaryaddition,subtraction, Multiplication, Division. **Complement of number:** Complements:1's,2's,9'sand10's. Subtraction using 1's and2's complement.	Interactive classroom lecture, PPT, demonstration, quiz, assignments, tutorial	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/assignments/ tutorial	3	2	Text Books, PPT, Handouts, chalk board, charts, Numerical Problems Workbook	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-02	Mid Semester Theory Exam	**Student will be asked to** (and/or): 1. Perform the given binary operation and complement of number/s.	10	Question paper, Rating scale	Internal

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)											
RGPV (Diploma Wing) Bhopal		**SCHEME FOR LEARNING OUTCOME**	**Branch Code**			**Course Code**			**CO Code**	**LO Code**	Format No. **4**
			E	0	3	3	0	3	1	3	
COURSE NAME	**Digital Electronics**										
CO Description	Examine the structure of various number system, codes and logic gates.										
LO Description	Verify truth table of all the gates.										

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-03	**Logic Gates:** Symbol, operation and truth-table: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR Realization of logic gates using universal gates. **Logic System:** Positive and negative logic system. Verification of the basic logic gates (AND, OR,NOT NAND , NOR ,EX-OR and EX-NOR).	Interactive classroom lecture, PPT , Lab demonstration, hands on practice, lab assignments.	• Teacher will explain the content in class/lab. • Teacher with support from lab staff will demonstrate the procedure of lab experiments. • Student will conduct lab assignment based on these experiments.	4	2	Text books, PPT, Lab manual, charts, Handouts, experimental trainer instruments/kit with measuring instruments, computer with relevant simulation software and high speed internet.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-03	End Semester Practical Exam	**Student will be asked to**(and/or): 1. Draw symbol and verify truth table of given logic gate. 2. Realization of gate using given universal gate	10	Rubrics, Rating scale	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)											
RGPV (Diploma Wing) Bhopal		**SCHEME FOR LEARNING OUTCOME**		**Branch Code**			**Course Code**			**CO Code**	**LO Code**	Format No. **4**
				E	0	3	3	0	3	2	4	
COURSE NAME	**Digital Electronics**											
CO Description	Construct and Examine simple combinational digital circuit.											
LO Description	VerifyBoolean algebra laws and theorems.											

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-04	**Laws and theorems of Boolean algebra:** Boolean laws, De-Morgan's Theorem and Duality Theorem, Complement of Boolean equations. Verification of De- Morgan's theorem.	Interactive classroom lecture, PPT , Lab demonstration, hands on practice, lab assignments.	• Teacher will explain the content in class/lab. • Teacher with support from lab staff will demonstrate the procedure of lab experiments. • Student will conduct lab assignment based on these experiments.	3	2	Text books, PPT, Lab manual, charts, Handouts, experimental trainer instruments/kit with measuring instruments, computer with relevant simulation software and high speed internet.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-04	Practical test in laboratory	**Student will be asked to**(and/or): 1. Explain given Boolean law and theorem. 2. Verify the De-Morgan's theorem.	10	Rubrics, Rating scale	Internal

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	0	3	3	0	3	2	5	

COURSE NAME	**Digital Electronics**
CO Description	Construct and Examine simple combinational digital circuit.
LO Description	Solve Boolean expressions using K-map and realize its logic circuit.

SCHEME OF STUDY

S. No.	Learning Content	Teaching –Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-05	**Karnaugh-map:** Boolean expressions: Sum of product and product of sum, Karnaugh maps and its use forsimplification up to four variable Boolean expressions, Don't care condition. **Realization of logic equations:** The universal building blocks- NAND & NOR, AND-OR network, NAND-NAND Logic for implementation of Boolean expressions.	Interactive classroom lecture, PPT, demonstration, quiz, assignments, tutorial	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/assignments/ tutorial	6	2	Text Books, PPT, Handouts, chalk board, charts, Numerical Problems Workbook	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-05	End Semester Theory Exam	**Student will be asked to** (and/or) 1. Simplify the Boolean expression using given method 2. Realize logic equation using given building block	10	Question paper, Rating scale	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	0	3	3	0	3	2	6	

COURSE NAME	**Digital Electronics**
CO Description	Construct and Examine simple combinational digital circuit.
LO Description	Implement different type of adder and subtractor circuits

SCHEME OF STUDY

S. No.	Learning Content	Teaching –Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-06	**Adder and Subtractor Circuit:** Half adder, full adder, parallel binary adder, 8421 adder, half subtractor, full subtractor, parallel binary subtractor.	Interactive classroom lecture, PPT, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/ assignments/ tutorial	4	1	Text Books, PPT, Handouts, chalk board, charts.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-06	End Semester Theory Exam	**Student will be asked to** 1. Explain the given adder and/or subtractor circuit.	10	Question paper, Rating scale	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	0	3	3	0	3	2	7	

COURSE NAME	**Digital Electronics**
CO Description	Construct and Examine simple combinational digital circuit.
LO Description	Design different type of coder and multiplexer circuits

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-07	**Coder Circuit:** Encoder, Decoder (2 to 4 line,3 to 8 line, BCD to Decimal, Decimal to7 segment) **MUX Circuit:** Multiplexers: 4 to1 and 8 to1. De-Multiplexers: 1 to 4 and 1 to 8. (Block Diagram & Truth table) Verification of encoder, decoder, multiplexer and de-multiplexer circuit.	Interactive classroom lecture, PPT , Lab demonstration, hands on practice, lab assignments.	• Teacher will explain the content in class/lab. • Teacher with support from lab staff will demonstrate the procedure of lab experiments. • Student will conduct lab assignment based on these experiments.	6	2	Text books, PPT, Lab manual, charts, Handouts, experimental trainer instruments/kit with measuring instruments, computer with relevant simulation software and high speed internet.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-07	Practical test in laboratory	**Student will be asked to**(and/or): 1. Explain the given coder or /and Mux circuit. 2. Verify the given Coder or/and Mux circuit.	10	Rubrics, Rating scale	Internal

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	0	3	3	0	3	3	8	

COURSE NAME	**Digital Electronics**
CO Description	Analyze flip-flop circuit, counters, shift registers and understand their operation.
LO Description	Analyze the working of various flip-flops and verify its outputs

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-08	**Flip-Flop:** S-R flip-flops(FF), D FF, Types of Triggering, Glitch, JK FF race around condition and remedies, JK Master Slave FF and T FF. Verification of various flip-flops	Interactive classroom lecture, PPT , Lab demonstration, hands on practice, lab assignments.	• Teacher will explain the content in class/lab. • Teacher with support from lab staff will demonstrate the procedure of lab experiments. • Student will conduct lab assignment based on these experiments.	5	3	Text books, PPT, Lab manual, charts, Handouts, experimental trainer instruments/kit with measuring instruments, computer with relevant simulation software and high speed internet.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal

LO-08	Practical test in laboratory	**Student will be asked to**(and/or): 1. Explain the given flip-flop circuit. 2. Verify the given flip-flop circuit.	10	Rubrics, Rating scale	Internal

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	*0*	*3*	*3*	*0*	*3*	*3*	*9*	

COURSE NAME	**Digital Electronics**
CO Description	Analyze flip-flop circuit, counters, shift registers and understand their operation.
LO Description	Draw and explain different type of registers

SCHEME OF STUDY

S. No.	Learning Content	Teaching –Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-09	**Registers:** Shift Register (3 to 4 bits only)- introduction, circuitdiagram and waveforms of SISO, SIPO,PISO, PIPO shift registers.	Interactive classroom lecture, PPT, demonstration, quiz, assignments, tutorial	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/assignments/ tutorial	4	1	Text Books, PPT, Handouts, chalk board, charts, Numerical Problems Workbook	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal

LO-09	End Semester Theory Exam	**Student will be asked to** 1. Draw circuit diagram and explain working with waveform of given register.	10	Question paper, Rating scale	External
ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)					

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	*0*	*3*	*3*	*0*	*3*	*3*	*10*	

COURSE NAME	**Digital Electronics**
CO Description	Analyze flip-flop circuit, counters, shift registers and understand their operation.
LO Description	Design different type of synchronous and asynchronous counters.

SCHEME OF STUDY

S. No.	Learning Content	Teaching – Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-10	**Counters:** Asynchronous: Up/down counters, Up-down counters. Synchronous Counters. Up/down counters, Ring counter, Johnson counter. Design Mode-4 counters.	Interactive classroom lecture, PPT , Lab demonstration, hands on practice, lab assignments.	• Teacher will explain the content in class/lab. • Teacher with support from lab staff will demonstrate the procedure of lab experiments. • Student will conduct lab assignment based on these experiments.	4	4	Text books, PPT, Lab manual, charts, Handouts, experimental trainer instruments/kit with measuring instruments, computer with relevant simulation software and high speed internet.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal

LO-10	End Semester Practical Exam	**Student will be asked to** 1. Design and explain the working of counter of given specification &/or type.	10	Rubrics/Rating scale	External
ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)					

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	*0*	*3*	*3*	*0*	*3*	*4*	*11*	

COURSE NAME	**Digital Electronics**
CO Description	Demonstrate the functioning of A to D and D to A Converters.
LO Description	Draw and explain various operation of D/A conversion circuits.

SCHEME OF STUDY

S. No.	Learning Content	Teaching –Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-11	**D/A Conversion**: Weighted resister, R-2R ladder network.	Interactive classroom lecture, PPT, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/ assignments/ tutorial	5	--	Text Books, PPT, Handouts, chalk board, charts.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-11	Mid Semester Theory Exam	**Student will be asked** **1.** Draw the circuit diagram and explain the working of given D/A converter.	10	Question paper, Rating scale	Internal
ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)					

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	0	3	3	0	3	4	12	

COURSE NAME	**Digital Electronics**
CO Description	Demonstrate the functioning of A to D and D to A Converters.
LO Description	Draw and explain various operation of A/D conversion circuits.

SCHEME OF STUDY

S. No.	Learning Content	Teaching –Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-12	**A/D Conversion:** Counter type, Successive approximation, Flash type, Dual slope type. (Theoretical aspects)	Interactive classroom lecture, PPT, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/ assignments/ tutorial	6	--	Text Books, PPT, Handouts, chalk board, charts.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-12	End Semester Theory Exam	**Student will be asked to** **1.** Draw the circuit diagram and explain the working of given A/D converter.	10	Question paper, Rating scale	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	SCHEME FOR LEARNING OUTCOME	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	0	3	3	0	3	5	13	

COURSE NAME	**Digital Electronics**
CO Description	Compare various digital logic family.

LO Description	Compare digital ICs on different parameters

SCHEME OF STUDY

S. No.	Learning Content	Teaching –Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-13	**Characteristics of digital ICs:** Fan-in, Fan-out, Propagation delay, Power dissipation, Noise margins, Figure of merit. **Logic ICs:** NAND Gate using TTL, NOR gate using ECL.	Interactive classroom lecture, PPT, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/ assignments/ tutorial	6	--	Text Books, PPT, Handouts, chalk board, charts.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-13	End Semester Theory Exam	**Student will be asked to (**and/or) 1. Characterize and compare the given digital IC/s. 2. Draw and explain the NAND/NOR gate using given logic ICs.	10	Question paper, Rating scale	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	0	3	3	0	3	5	14	

COURSE NAME	Digital Electronics
CO Description	Compare various digital logic family.
LO Description	Construct universal gates and inverter using MOS and CMOS logic

SCHEME OF STUDY

S. No.	Learning Content	Teaching –Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks
LO-14	**Classifications of logic families:** Saturated and Non-saturated logic. **MOS and CMOS Logic:** MOS based NOT gate, Two input NAND & NOR gate. CMOS based NOT gate, Two input NAND & NOR gate.	Interactive classroom lecture, PPT, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/ assignments/ tutorial	6	--	Text Books, PPT, Handouts, chalk board, charts.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-14	End Semester Theory Exam	**Student will be asked to (**and/or) 1. Classify the logic families. 2. Design universal and inverter gate using given logic family.	10	Question paper, Rating scale	External

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)

RGPV (Diploma Wing) Bhopal	**SCHEME FOR LEARNING OUTCOME**	Branch Code			Course Code			CO Code	LO Code	Format No. **4**
		E	*0*	*3*	*3*	*0*	*3*	*5*	*15*	

COURSE NAME	**Digital Electronics**
CO Description	Compare various digital logic family.
LO Description	Make use of PAL & PLA for implementation of Boolean expression and design simple logic circuit.

SCHEME OF STUDY

S. No.	Learning Content	Teaching –Learning Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Required	Remarks

LO-15	**PLD:** PAL, PLA Implementation of Boolean expression using PAL, PLA (Up-to 2 variables)	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/ assignments/ tutorial	6	--	Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.	

SCHEME OF ASSESSMENT

S. No.	Method of Assessment	Description of Assessment	Maximum Marks	Resources Required	External / Internal
LO-15	Seminar presentation	**Student will be asked to** 1. Present on given PLA &/or PAL 2. Implement given Boolean expression using PAL/PLA	10	Rubrics, Rating scale	Internal

ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)