RGF WI	PV (D NG) e	iplom Bhopa	A L	OBE CURR THE	RICULUM FO	FORMAT-		Sh No	neet 5. 1/5				
Branch		E	lectron	ics & Tele-commu	nication	5	Semester		3	3			
Course (Code			Course Name Digital Electronics									
Course Outcome 1			Exami and lo	ne the structure of gic gates.	various number sy	rstem	, codes	Tead Hrs	ch s	Marks			
Learning	g Outc	ome 1	List ou conve	It different types o rt one to another.	f number system & (Cognitive)	code	and	8		10			
Co	ontent	S	Number System: Decimal number, binary number, octal and Hexadecimal number. Binary Codes: Weighted and un-weighted codes BCD, Gray, Excess-3. Conversion of number system and code: (Decimal number, binary number, octal and Hexadecimal number, BCD, Gray, Excess-3)										
Method	of Asse	ssment	Exterr	al									
Learning	g Outc	ome 2	Perform various binary arithmetic operation. (Cognitive)510										
Co	ontent	S	Binary operations: Binaryaddition, subtraction, Multiplication, Division. Complement of number: Complements: 1's,2's,9'sand10's. Subtraction using 1's and2's complement.										
Method	of Asse	ssment	Intern	al									
Learning	g Outo	ome 3	Verify	truth table of all th	ne gates. (Psychom	otor)		6		10			
Contents Logic Gates: Symbol, operation and truth-table: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR Realization of logic gates using universal gates. Logic System: Positive and negative logic system. Verification of the basic logic gates (AND, OR, NOT NAND , N NOR).								,EX-C)R ai	nd EX-			
Method	of Asse	ssment	Extern										

RGPV (WING)	DIPLOM BHOPA	A L	OBE CURR THE	RICULUM FOR COURSE	FORMA	r ₋3	Sheet No. 2/5						
Branch	E	Electron	ics & Tele-commu	nication	Semester		3						
Course Code	9		Course Name	S									
Course Out	tcome 2	Const circuit	ruct and Examine s	imple combinational d	igital	Teac Hrs	h Marks						
Learning Ou	itcome 4	Verify (Psych	Boolean algebra la homotor)	aws and theorems.		5	10						
Conte	nts	Laws Boolea Boolea Verific	Laws and theorems of Boolean algebra: Boolean laws, De-Morgan's Theorem and Duality Theorem, Complement of Boolean equations. Verification of De- Morgan's theorem.										
Method of As	sessment	Intern	al										
Learning Ou	itcome 5	Solve logic c	Solve Boolean expressions using K-map and realize its810logic circuit. (Cognitive)10										
Conte	nts	Karna Boolea its use condit Reali The Logic f	augh-map: an expressions: Sum forsimplification up ion. zation of logic equa e universal building for implementation	of product and produc to four variable Boolea ations: blocks-NAND & NOR, Al of Boolean expressions.	t of sum, Karı ın expression ND-OR netwo	naugh s, Don ork, NA	maps and 't care ND-NAND						
Method of As	sessment	Extern	al										
Learning Ou	Itcome 6	Imple (Cogn	ment different type itive)	e of adder and subtract	tor circuits.	5	10						
Conte	nts	Adder and Subtractor Circuit: Half adder, full adder, parallel binary adder, 8421 adder, half subtractor, full subtractor, parallel binary subtractor.											
Method of As	sessment	Exterr	nal										
Learning Ou	itcome 7	Desigr (Psych	Design different type of coder and multiplexer circuits810(Psychomotor)10										
Conte	nts	Code E (2 MUX M D	er Circuit: Encoder, Decoder 2 to 4 line,3 to 8 line 3 Circuit: Iultiplexers: 4 to1 an e-Multiplexers: 1 to	e, BCD to Decimal, Deci nd 8 to1. 9 4 and 1 to 8.	mal to7 segm	ient)							

	(Block Diagram and Truth table) Verification of encoder, decoder, multiplexer and de-multiplexer circuit.
Method of Assessment	Internal

RGPV (D WING) E	iplom Bhopa	A L	OBE CURR THE	RICULUM FOR COURSE	FORMAT	.3	Sł No	Sheet No. 3/5				
Branch	E	lectron	ics & Tele-commur	nication	S	emester			3			
Course Code			Course Name	Ime Digital Electronics								
Course Outco	ome 3	Analyz under	ze flip-flop circuit, c stand their operati	ounters, shift register on.	's a	nd	Teach Hrs.		Marks			
Learning Outo	come 8	Analyz outpu	ze the working of va ts. (<i>Psychomotor</i>)	arious flip-flops and ve	erif	y its	8		10			
Content	S	Flip-Flop: S-R flip-flops(FF), D FF, Types of Triggering, Glitch, JK FF race around condition and remedies, JK Master Slave FF and T FF. Verification of various flip-flops										
Method of Asse	essment	Intern	al									
Learning Outo	come 9	Draw	and explain differe	nt type of registers. (C	Cog	nitive)	5		10			
Content	S	Registers: Shift Register (3 to 4 bits only)- introduction, circuitdiagram and waveforms of SISO, SIPO, PISO, PIPO shift registers.										
Method of Asse	essment	Exterr	nal									
Learning Out 10	come	Design different type of synchronous and asynchronous810counters. (Psychomotor)10										
Content	S	Coun Asy Up/ Syn Up/ Desig	Counters: Asynchronous: Up/down counters, Up-down counters. Synchronous Counters. Up/down counters, Ring counter, Johnson counter. Design Mode-4 counters.									
Method of Asse	essment	Extern	nal									

RGPV (DIPLOMA WING) BHOPAL				OBE CURR THE	RICULUM FOR	FORMA	r- 3	Sheet No. 4/5		
Branch		E	lectron	ics & Tele-commur	nication	Semester		3		
Course	Code			Course Name	Digit	al Electronic	S			
Course Outcome 4			Demo Conve	nstrate the functio rters.	ning of A to D and D to	A	Tead Hrs	ch Marks		
Learnir	ng Out 11	come	Draw circuit	and explain various s. (<i>Cognitive)</i>	s operation of D/A con	version	5	10		
Co	ontent	S	D/A (Weigh	C onversion: ted resister, R-2R lad	der network.		1			
Method	of Asse	essment	Intern	al						
Learnir	ng Out 12	come	Draw circuit	Draw and explain various operation of D/A conversion610circuits. (Cognitive)6						
Co	ontent	S	A/D Counter type.(T	Conversion: er type, Successive ap Theoretical aspects)	pproximation, Flash type,	, Dual slope	1	,		
Method	of Asse	essment	Exterr	al						

RGPV	(DIPL(BHO	oma Wing) Pal	OBE CURF THE	RICULUM FOR COURSE	FORMA	FORMAT-3		
Branch		Electron	ics & Tele-commu	nication	Semester		3	
Course Code		Course Name	Digita	al Electronics	5			

Course Outcome 5	Compare various digital logic family.	Teach Hrs.	Marks							
Learning Outcome 13	Compare digital ICs on different parameters. (Cognitive)	6	10							
Contents	Characteristics of digital ICs: Fan-in, Fan-out, Propagation delay, Power dissipation, Noise margins, Figure of merit. Logic ICs: NAND Gate using TTL, NOR gate using ECL.									
Method of Assessment	External									
Learning Outcome 14	Construct universal gates and inverter using MOS and CMOS logic. (<i>Cognitive</i>)	6	10							
Contents	 Classifications of logic families: Saturated and Non-saturated logic. MOS and CMOS Logic: MOS based NOT gate, Two input NAND & NOR gate. CMOS based NOT gate, Two input NAND & NOR gate. 		1							
Method of Assessment	External									
Learning Outcome 15	Make use of PAL & PLA for implementation of Boolean expression and design simple logic circuit. (<i>Cognitive/Affective</i>)	6	10							
Contents	PLD: PAL,PLA Implementation of Boolean expression using PAL,PLA (Up-to 2 variables)									
Method of Assessment	Internal									

Suggested Experiment:

S. No.	Practical Experiment	СО
1.	Verify the basic logic gates (AND, OR,NOT NAND, NOR	CO302.2
	,EX-OR and EX-NOR).	
2.	Verify De- Morgan's theorem.	CO302.2
3.	Verify half adder and full adder circuit using EX-OR, AND,	CO302.2
	OR logic gates.	

4.	Verify half subtractor, full subtractor circuit using EX-OR,	CO302.2
	AND, OR logic gates.	
5.	Verify parallel binary subtractor circuit.	CO302.2
6.	Verify 4 bit parallel adder circuit.	CO302.2
7.	Verify the 2 to 4 or 3 to 8 lines decoder circuit.	CO302.2
8.	Verify BCD to 7 segment decoder circuit.	CO302.2
9.	Verify the encoder circuit.	CO302.2
10.	Realize the minimized network of a given function and verify truth table.	CO302.2
11.	Verify the 4:1 or 8:1, multiplexer circuit.	CO302.2
12.	Verify the 1:4 or 1:8 de multiplexer circuit.	CO302.2
13.	Verify SR flip-flop and construct D flip-flop from it.	CO302.3
14.	Verify JK flip-flop and constructT flip-flop from it.	CO302.3
15.	Verify JK master slave flip-flop.	CO302.3
16.	Design Mode-4 Counters.	CO302.3
17.	Design and Develop mini project using digital logic.	CO302.2,
		CO302.3,
		CO302.4

Suggestions:

Experiments are expected to be performed

- 1. Using breadboard/trainer kits.
- 2. Simulation software (anyone like: PSpice, TINA, Multisim, KiCAD, LTSpice, LabView, Simulink, Proteus, CircuitMaker etc.)
- 3. On virtual lab platforms available online (like: vlab.co.in, falstad.com/circuit etc.)

SuggestedActivities:

- 1. Interpret any one DataSheet of A to D or D to A Converter. (CO302.4)
- 2. List at least two IC's per Logic Family. (CO302.5)

LEARNING RESOURCES:

Reference Books:

S. No	Title of Book	Author	Publication				
1.	Fundamentals of Digital	A. Anand Kumar	PHI, 2009 or latest				
	Circuits						
2.	Digital Electronics and Logic	Sharma Sanjay	S. K. Kataria& Sons,				
	Design		2012 or latest				
3.	Modern Digital Electronics	Jain R P	TMH, 2009 or latest				
4.	Digital Electronics	K. Meena	PHI, 2009 or latest				
5.	Digital Electronics Principles	Malvino& Leach	TMH, 2011 or latest				
6.	Digital Electronics	Morris Mano	Pearson, 2008 or latest				
7.	Digital Fundaments	Floyd Thomas L & Jain	Pearson, 2011 or latest				
8.	Digital Electronics	Shiv Shankar Mishra	Satya Prakashan New Delhi				

List of Software/Learning Websites:

- 1. www.nptel.iitm.ac.in
- 2. www.ocw.mit.edu
- 3. www.slideshare.net

	PCDV (Diploma Wing) Phona			SCHEME FOR LEARNING				Branch	Code		Course Co	Course Code CO Coc			/
KGPV		ma wing) b	nopai	OUTCOME			Ε	0) 3	3	0	3	1	1	Format No. 4
COURS	E NAME	Digital Electroni	ics												
CO Des	cription	Examine the struct	ure of vario	us number syste	m, codes and logic gates.										
LO Des	cription	List out different ty	pes of num	ber system & co	de and convert one to ano	ther.									
					SCHEME OF STU	DY									
S. No.	Lear	ning Content	Teachii N	ng –Learning 1ethod	Description of T-L Process	Teac Hrs	:h :.	Pr /Tu	act. t Hrs.		LRs Re	equir	ed		Remarks
LO-01 Number System: Decimal number, binary number, octal and Hexadecimal number. Binary Codes: Weighted and un-weighted codes BCD, Gray, Excess-3. Conversion of number system and code: (Decimal number, binary number, octal and Hexadecima			Interactive classroom Telecture, PPT, the demonstration, quiz, pressignments, tutorial st Televas tu		Teacher will explain the contents and provide handouts to students. Teacher will conduct assignments/ quiz/ tutorial	5		3		Text Books, PPT, Handouts, chalk board, charts. Numerical Proble Workbook		ooks, PPT, outs, chalk , charts. rical Problems oook			
					SCHEME OF ASSESS	MENT									
S. No.	Method	of Assessment		Descrip	otion of Assessment				Ma m N	ximu 1arks	Res	ource	es Req	uired	External / Internal
LO-01 End Semester Theory Exam Exam 2. Convert give				vill be asked to n the given nu rt given numb	be asked to (and/or) he given number system or binary code. given number system/ binary code to another.			10			Question paper, Rating scale		er,	External	
	1		AD	DITIONAL INS	TRUCTIONS FOR THE	HOD/	FAC	CULT	Y (IF A	NY)					1

RGP	/ (Diplo	oma Wing) Bh	nopal	SCHEM	E FOR LEAR	RNING	G	Branch Code	C	Course Code		CO Code	LO Code	Format No. 4
		- J,			OUTCOME		E	: 0 3	3	0	3	1	2	
COURS	SE NAME	Digital Electronics												
CO Description Examine the structure of various number system, codes and logic gates.														
LO Des	Description Perform various binary arithmetic operation.													
					SCHEME C	F STUE	Ŋ							
S. No.	No. Learning Content		Teachir N	ng –Learning 1ethod	of T-L	Teach Hrs.	Pract. /Tut Hrs.	LRs Required				Remarks		
LO-02	LO-02 Binary operations: Binaryaddition, subtractio n, Multiplication, Division. Complement of number: Complements: 1's,2's,9'san d10's. Subtraction using 1's and2's		Interacti lecture, l demonst assignme	ve classroom PPT, tration, quiz, ents, tutorial	the contents and provide handouts to students. Teacher will conduct quiz/assignments/ tutorial		3	2	Handouts, chalk board, charts, Numerical Problems Workbook					
					SCHEME OF A	SSESSI	MENT							
S. No. Method of Assessment Description of As			Assessment Maximu Marks			Resources Required						External / Internal		
LO-02 Mid Semester Theory Exam ^{1.}			Stude 1. Per ope nur	nt will be aske form the give eration and co mber/s.	10 Quest			stion paper, Rating scale					Internal	

			AD	DITIONAL	INSTRUCTIONS FOR THE I	HOD/F/	ACULTY (IF A	NY)			
RGP	/ (Diplo	oma Wing) B	hopal	SCHE	ME FOR LEARNING OUTCOME	G	Branch Code	Course Code	CO Code	LO Code 3	Format No. 4
COURS	J (Diploma VVing) SE NAME Digital Electr Scription Examine the str Scription Verify truth tab Learning Content Logic Gates: Symbol, operation and truth table: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR Realization of logic gates using universal gates. Logic System:Positive and		CS								
CO Des	cription	Examine the structu	ure of variou	us number sy	stem, codes and logic gates.						
LO Des	cription	Verify truth table o	f all the gate	es.							
					SCHEME OF STUE	ΟY					
S. No.	Lear	ning Content	Teac Learnin	hing – g Method	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs Requir	ed		Remarks
LO-03	LO-03 Logic Gates: Symbol, operation and truth- table: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR Realization of logic gates using universal gates. Logic System:Positive and negative logic system. Verification of the basic logic gates (AND, OR,NOT NAND, NOR ,EX-OR and EX-NOR).		Interactiv classroor PPT , La demonst hands or lab assig	re n lecture, b ration, n practice, nments.	 Teacher will explain the content in class/lab. Teacher with support from lab staff will demonstrate the procedure of lab experiments. Student will conduct lab assignment based on these experiments. 	4	2	Text books, PP manual, charts Handouts, experimental t instruments/ki measuring instruments, computer with relevant simula software and h speed internet	т, Lab rainer t with ation igh		
					SCHEME OF ASSESS	MENT					
S. No.	Metho	d of Assessment		Descrip	otion of Assessment		Maximum Marks	Resources	Requ	ired	External / Internal
LO-03	End Se	emester Practical Exam	Student 1. Draw logic 2. Realiz	will be asl symbol an gate. zation of ga	k ed to (and/or): Id verify truth table of given The using given universal g	en gate	10	Rubrics, R	ating s	cale	External

			ADI	DITIONAL	INSTRUCTIONS FOR THE HO	D/ FACL	JLTY (IF AN	Y)							
RGPV	(Diplo	oma Wing)	Bhopal	SCHI	EME FOR LEARNING OUTCOME	Bra	anch Code	Course Code	CO Code 2	LO Code 4	Format No. 4				
COURS	E NAME	Digital Electro	nics												
CO Des	cription	Construct and Exa	amine simple (combinatio	nal digital circuit.										
LO Desc	cription	VerifyBoolean alg	gebra laws and	theorems											
		1			SCHEME OF STUDY										
S. No.	No. Learning Content Teaching – Learning Method Description of T-L Process Teach Hrs. Pract. /Tut Hrs. LRs Required Remarks -04 Laws and theorems of Boolean algebra: Interactive classroom lecture • Teacher will explain the content in class (/sh 3 2 Text books, PPT, Lab														
LO-04	O-04 Laws and theorems of Boolean algebra: Boolean laws, De-Morgan's Theorem and Duality Theorem, Complement of Boolean equations. Verification of De- Morgan's theorem.			ecture, on, ractice, nents.	 Teacher will explain the content in class/lab. Teacher with support from lab staff will demonstrate the procedure of lab experiments. Student will conduct lab assignment based on these experiments. 	3	2	Text books, F manual, char Handouts, ex trainer instru- with measur instruments, with relevant software and internet.	PPT, La tes, iments ing compu t simul I high s	b ental /kit uter ation peed					
	1				SCHEME OF ASSESSME	NT									
S. No.	Metho	od of Assessmer	nt	Desc	ription of Assessment		Maximum Marks	Resource	s Requ	ired	External / Internal				
LO-04	Practica	l test in laborate	ory 1. Exp 2. Ve	nt will be plain give crify the D	asked to (and/or): n Boolean law and theorem. e-Morgan's theorem.		10	Rubrics, F	Rating s	scale	Internal				
	1		ADI	DITIONAL	INSTRUCTIONS FOR THE HO	D/ FACL	JLTY (IF AN	Y)			1				

	/Dinla		anal	SCHEM	E FOR LEARNING	3	Br	ranch Cod	e	C	ourse Co	de	CO Code	LO Code	
KGPV		oma wing) Br	iopai		OUTCOME		E	0	3	3	0	3	2	5	Format No. 4
COURS	E NAME	Digital Electronics	S								_				1
CO Dese	cription	Construct and Exami	ne simple	combinational c	ligital circuit.										
LO Desc	cription	Solve Boolean expres	ssions usir	ng K-map and rea	alize its logic circuit.										
					SCHEME OF STUE	ΟY									
S. No.	Lear	ning Content	Teachir N	ng -Learning 1ethod	Description of T-L Process	Teacl Hrs.	n /	Pract /Tut H	t. rs.	L	.Rs Re	quir	ed		Remarks
LO-05	Karnaugh Boolean e product ar Karnaugh forsimplifi variable B Don't care Realization The univer NAND & N network, I for implen expression	n-map: xpressions: Sum of nd product of sum, maps and its use cation up to four oolean expressions, e condition. n of logic equations: rsal building blocks- IOR, AND-OR NAND-NAND Logic nentation of Boolean ns.	Interacti lecture, l demonst assignme	ve classroom PPT, tration, quiz, ents, tutorial	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/assignments/ tutorial	6		2		Text Hanc board Num Work	Books louts, d, cha erical ‹book	s, PPT chalk rts, Probl	ems		
		!			SCHEME OF ASSESS	MENT									
S. No.	Metho	od of Assessment		Descriptio	on of Assessment		Ν	Maxim Mark	ium <s< th=""><th></th><th>Reso</th><th>urces</th><th>Requ</th><th>ired</th><th>External / Internal</th></s<>		Reso	urces	Requ	ired	External / Internal
LO-05	End Sen	nester Theory Exam	Studer 1. Sim me 2. Rea bloo	nt will be asked aplify the Book thod alize logic equa ck	l to (and/or) ean expression using g ation using given buildi	iven ng		10		(Questi	on pa sca	per, R Ile	ating	External
			AD	DITIONAL INS	TRUCTIONS FOR THE	HOD/ F	ACL	ULTY (if an	IY)					·

	(Dinlo	ma Wing) Bl	nonal	SCHEM	E FOR LEAR	NIN	G	Branch Code	Course	e Code	CO Code	LO Code		
NOF V		ina wing j bi	ισμαι	(OUTCOME		E	E 0 3	3 (0 3	2	6	Format No. 🛥	
COURS	E NAME	Digital Electronic	s											
CO Des	cription	Construct and Exam	ine simple	combinational d	ligital circuit.									
LO Desc	cription	Implement different	type of ac	lder and subtrac	tor circuits									
	SCHEME OF STUDY													
S. No.	No.Learning ContentTeaching –Learning MethodDescription of T-L ProcessTeach Hrs.Pract. /Tut Hrs.LRs RequiredRemarks													
LO-06	Adder an Circu Half adder binary add subtractor parallel bin	nd Subtractor nit: 7, full adder, parallel der, 8421 adder, half 7, full subtractor, nary subtractor.	Interactiv lecture, f demonst assignme	ve classroom PPT, tration, quiz, ents.	Teacher will exp the contents an provide handou students. Teach will conduct qui assignments/ tu	olain d its to ier iz/ itorial	4	1	Text Boo Handou board, c	oks, PPT, ts, chalk harts.	,			
					SCHEME OF A	SSESSI	MENT							
S. No.	Metho	d of Assessment	De	escription of A	ssessment	Max M	kimum arks	R	esources	Require	ed		External / Internal	
LO-06	End Sen	nester Theory Exam	Studer 1.	it will be asked Explain the gi and/or subtra	l to iven adder actor circuit.		10	Ques	tion pape	r, Rating	g scale		External	
			AD	DITIONAL INS	TRUCTIONS FO	R THE	HOD/ FA	CULTY (IF A	NY)					

	/ (Dinla	ma Wing) Dk	onal	SCHE	EME FOR LEARNING	G	Branch C	ode	(Course Co	ode	CO Code	LO Code	
KGPV		oma wing) Br	юраі		OUTCOME		E 0	3	3	0	3	2	7	Format No. 4
COURS	E NAME	Digital Electronics	S			'								
CO Des	cription	Construct and Exami	ne simple c	combinatio	nal digital circuit.									
LO Des	cription	Design different type	e of coder a	and multipl	exer circuits									
					SCHEME OF STUE	ΟY								
S. No.	Lear	ning Content	Teach Learr Metl	ling – ning hod	Description of T-L Process	Teach Hrs.	Pra /Tut	ct. Hrs.		LRs R	equir	ed		Remarks
LO-07	LO-07 Coder Circuit: Encoder, Decoder (2 to 4 line,3 to 8 line, BCD to Decimal, Decimal to7 segment) MUX Circuit: Multiplexers: 4 to1 and 8 to1. De-Multiplexers: 1 to 4 and 1 to 8. (Block Diagram & Truth table) Verification of encoder, decoder, multiplexer and de- multiplexer circuit.				 Teacher will explain the content in class/lab. Teacher with support from lab staff will demonstrate the procedure of lab experiments. Student will conduct lab assignment based on these experiments. 	6	2		Text man Han expe instr mea instr with simu and inter	books ual, cl douts, erimer rumen suring rumen relev ulatior high s rnet.	s, PPT narts, ntal tra ts/kit ts, coi ant softw peed	, Lab ainer with mputer vare	r	
					SCHEME OF ASSESS	MENT								
S. No.	Metho	od of Assessment		Desci	ription of Assessment		Max Ma	imun arks	n	Reso	urces	Requ	ired	External / Internal
LO-07	Practica	l test in laboratory	Studen 1. Expla 2. Verif	t will be a ain the gi fy the give	asked to (and/or): ven coder or /and Mux circ en Coder or/and Mux_circ	cuit. uit.		10		Rubr	ics, R	ating s	cale	Internal
			ADD	DITIONAL	INSTRUCTIONS FOR THE	HOD/ F	ACULTY	(IF A	NY)					

	/ (Diplo	ma Wing) Pl	honal	SCHEI	ME FOR LEAR	NING		Branch Coo	le	Co	ourse Co	de	CO Code	LO Code	
KUPV		illa vviliy) di	порат		OUTCOME		E	0	3	3	0	3	3	8	Format No. 4
COURS	E NAME	Digital Electronic	S												
CO Des	cription	Analyze flip-flop circ	cuit, counte	ers, shift regis	ters and understand tl	heir oper	ation.								
LO Des	cription	Analyze the working	g of various	flip-flops and	l verify its outputs										
	SCHEME OF STUDY Teaching – Description of T-L Teach Pract.														
S. No.	Lear	ning Content	Teac Learnin	:hing – g Method	Description of Process	T-L	Teach Hrs.	Prac /Tut F	t. Irs.	L	Rs Re	quir	ed		Remarks
LO-08	Flip-Flop S-R flip- Types of Glitch, JK FF ra condition JK Mast	eflops(FF), D FF, Triggering, ace around and remedies, ter Slave FF and T FF. n of various flip-flops	Interactiv classroor PPT , Lab demonst hands on lab assign	ve n lecture, ration, n practice, nments.	 Teacher will explating the content in class/lab. Teacher with sup from lab staff will demonstrate the procedure of lab experiments. Student will conduct lab assignment be on these experiments. 	ain pport I duct ased nents.	5	3		Text I manu Hand exper instru meas instru with simul and h interr	books Jal, ch outs, rimen Jumen Jumen Jumen releva Jation Jation Jation Jation	s, PPT harts, tal tra ts/kit ts, col ant softv peed	, Lab ainer with mpute vare	r	
					SCHEME OF AS	SSESSM	ENT								
S. No.	Metho	d of Assessment	De	scription o	f Assessment	Maxii Ma	mum rks		Re	sourc	es Re	equir	ed		External / Internal

LO-08	Practica	l test in laboratory	Stude 1. Exp circ 2. Ver	nt will be aske blain the given cuit. rify the given f	e d to (and/or): flip-flop lip-flop circuit.	1	10	R	ubrics,	Ratii	ng sca	le		Internal
	1		AD	DITIONAL INS	TRUCTIONS FO	R THE F	HOD/F/	ACULTY (IF A	NY)					1
	(Dinlo	ma Wing) Bh	onal	SCHEM	E FOR LEAR	NING	3	Branch Code	Coι	urse Co	de	CO Code	LO Code	
			iopai		OUTCOME			E 0 3	3	0	3	3	9	Format No. 🛥
COURS	E NAME	Digital Electronics	S											
CO Des	cription	Analyze flip-flop circu	uit, counte	ers, shift register	s and understand t	heir ope	ration.							
LO Desc	cription	Draw and explain dif	ferent typ	e of registers										
		·			SCHEME O	F STUD	γ							
S. No.	Lear	ning Content	Teachii N	ng -Learning Nethod	Description o Process	of T-L	Teach Hrs.	Pract. /Tut Hrs.	LF	Rs Re	equire	ed		Remarks
LO-09	Registers Shift Regi introducti and wave SIPO,PISC registers.	: ster (3 to 4 bits only)- ion, circuitdiagram forms of SISO,), PIPO shift	Interacti lecture, demons assignm	ve classroom PPT, tration, quiz, ents, tutorial	Teacher will exp the contents an provide handou students. Teach will conduct quiz/assignmen tutorial	olain d its to ier ts/	4	1	Text B Hando board Nume Workb	Books Duts, I, cha Prical book	s, PPT, chalk rts, Proble	ems		
		· · ·			SCHEME OF A	SSESSN	/IENT							
S. No.	Metho	od of Assessment	De	escription of A	ssessment	Max Ma	imum arks	R	esource	es Re	equire	ed		External / Internal

LO-09	End Sem	nester Theory Exam	Student will be asl 1. Draw circu explain wo waveform	ked to lit diagram and orking with of given register.	10		Quest	ion paper, Rating	g scale		External
			ADDITIONAL	NSTRUCTIONS FO	R THE HOI	D/ FA	CULTY (IF AI	NY)			·
RGPV	' (Diplo	oma Wing) Bł	nopal SCHE	ME FOR LEAR OUTCOME	NING	E	Branch Code	Course Code	CO Code 3	LO Code 10	Format No. 4
COURS	E NAME	Digital Electronic	S				I I			1	·
CO Des	cription	Analyze flip-flop circ	uit, counters, shift regis	sters and understand t	heir operati	ion.					
LO Desc	cription	Design different type	e of synchronous and as	synchronous counters							
				SCHEME O	F STUDY						
S. No.	Lear	ning Content	Teaching – Learning Method	Description of Process	T-L Te	each Irs.	Pract. /Tut Hrs.	LRs Requi	red		Remarks
LO-10	Counters Asynchr Up/do Up-d Synch Coun Up/do counter, Design N	: onous: wn counters, lown counters. ronous hters. wn counters, Ring Johnson counter. Mode-4 counters.	Interactive classroom lecture, PPT , Lab demonstration, hands on practice, lab assignments.	 Teacher will expl the content in class/lab. Teacher with sup from lab staff will demonstrate the procedure of lab experiments. Student will cond lab assignment b on these experiments 	ain oport II duct based hents.	4	4	Text books, PPT, manual, charts, Handouts, exper trainer instrume with measuring instruments, cor with relevant sir software and hig internet.	Lab imenta nts/kit nputer nulatio gh spee	al	
				SCHEME OF A	SSESSME	NT	1				1
S. No.	Metho	d of Assessment	Description o	f Assessment	Maxim Mark	um s	Re	esources Require	ed		External / Internal

LO-10	End S	emester Practio Exam	cal 1	Student will Design an counter o &/or type	II be as nd expla of given e.	sked to ain the working of a specification	10		Rubr	ics/Rating sca	lle		External
				ADDITIO	ONAL I	NSTRUCTIONS FO	R THE HOD	/ FACUL	TY (IF ANY)				
RGPV	/ (Diplo	ma Wing)) Bho	pal S(CHEI	ME FOR LEAR OUTCOME	NING	Brand	ch Code	Course Code	CO Code 4	LO Code 11	Format No. 4
COURS	E NAME	Digital Electr	onics					<u> </u>	· ·	· · ·			·
CO Des	cription	Demonstrate th	ne functio	oning of A to I	D and D	D to A Converters.							
LO Desc	cription	Draw and expla	ain variou	us operation o	of D/A c	conversion circuits.							
	SCHEME OF STUDY												
S. No.	Learni	ng Content	Teac	hing –Learn Method	ning	Description o Process	of T-L	Teach Hrs.	Pract. /Tut Hrs.	LRs Requ	uired		Remarks
LO-11	D/A Con Weighted 2R ladder	version: I resister, R- ⁻ network.	Interac lecture demor assignr	ctive classroc e, PPT, nstration, qui ments.	om Jiz,	Teacher will explai contents and provi handouts to stude Teacher will condu assignments/ tuto	n the ide nts. ıct quiz/ rial	5		Text Books Handouts, board, cha	, PPT, chalk rts.		
						SCHEME OF A	SSESSMEN ⁻	Г					
S. No.	Metho	d of Assessme	ent	D	Descrip	tion of Assessmer	nt	Ma	aximum Marks	Resources	Requ	ired	External / Internal
LO-11	Mid Seme	ester Theory Ex	sam s	Student will 1. Draw worki	l be ask v the cir king of (ced rcuit diagram and ex given D/A converter	xplain the		10	Question past sc	aper, R ale	ating	Internal
	<u>.</u>		I	ADDITIO	ONAL I	NSTRUCTIONS FO	R THE HOD	/ FACUL	TY (IF ANY)				·

RGPV	/ (Diplo	ma Wing) Bł	nopal	SCHEM (E FOR LEAR OUTCOME	NINC) 	Branch Code	3 3	Course Code	CO Code 4	LO Code 12	Format No. 4
COURS	E NAME	Digital Electronic	S						I			1	
CO Des	cription	Demonstrate the fur	nctioning c	of A to D and D to	A Converters.								
LO Desc	cription	Draw and explain va	rious oper	ation of A/D con	version circuits.								
		·			SCHEME O	F STUE	ŊΥ						
S. No.	Lear	ning Content	Teachir N	ng -Learning 1ethod	Description o Process	f T-L	Teach Hrs.	Pract. /Tut Hrs.		LRs Requir	ed		Remarks
LO-12	A/D Com Counter approxim Dual slop (Theoreti	version: type, Successive nation, Flash type, e type. cal aspects)	Interacti lecture, I demonst assignme	ve classroom PPT, tration, quiz, ents.	Teacher will exp the contents and provide handou students. Teach will conduct qui assignments/ tu	olain d ts to er z/ torial	6		Text Hand boar	Books, PPT douts, chalk d, charts.			
					SCHEME OF AS	SSESSN	/ENT						
S. No.	Metho	d of Assessment	De	escription of A	ssessment	Max Ma	imum arks		Resour	ces Requir	ed		External / Internal
LO-12	End Sem	nester Theory Exam	Studer 1. Dr ex co	nt will be asked raw the circuit of plain the worki poverter.	l to diagram and ng of given A/D		10	Que	stion p	aper, Rating	g scale		External
			AD	DITIONAL INS	TRUCTIONS FOR	R THE I	HOD/ FA	ACULTY (IF)	ANY)				
	//D:!-			SCHEM	E FOR LEAR	NINC	3	Branch Code	(Course Code	CO Code	LO Code	Л
KGPV		ma wing) Bi	nopal	(OUTCOME		E	E 0 3	3 3	0 3	5	13	Format No. 4
COURS	E NAME	Digital Electronic	S				`	· ·		· ·			
CO Des	cription	Compare various dig	jital logic f	amily.									

LO Desc	cription	Compare digital ICs	on different parar	neters										
					SCHEME OF STU	ΟY								
S. No.	Lear	ning Content	Teaching –Le Methoo	arning 1	Description of T-L Process	Teach Hrs.	Pract. /Tut Hrs.	LRs R	equir	ed		Remarks		
LO-13	Characte digital IC Fan-i Propa Powe Noise Figur Logio NAND Gate using ECL.	eristics of Cs: n, Fan-out, agation delay, r dissipation, e margins, e of merit. e ICs: e using TTL, NOR gate	Interactive clas lecture, PPT, demonstration assignments.	sroom , quiz,	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/ assignments/ tutorial	6		Text Book Handouts board, ch	s, PPT , chalk arts.	,				
	using ECL. SCHEME OF ASSESSMENT													
S. No.	SCHEME OF ASSESSMENT No. Method of Assessment Maximum Marks Resources Required External / Internal													
LO-13	End Sem	nester Theory Exam	Student will I 1. Character 2. Draw and given logi	be asked rize and I explain c ICs.	l to (and/or) compare the given dig the NAND/NOR gate (ital IC/s. Jsing	10	Que	stion p sc	aper, R ale	ating	External		
	1		ADDITIO	NAL INS	TRUCTIONS FOR THE	HOD/ FA	CULTY (IF A	NY)				I		
			S	CHEM	E FOR LEARNING	3	Branch Code	Course (ode	CO Code	LO Code			
RGPV	(Dibio	ma wing) Br	nopai	(OUTCOME	E	03	3 0	3	5	14	Format No. 4		
COURS	E NAME	Digital Electronic	S			I	I	I						
CO Des	cription	Compare various dig	ital logic family.											
LO Desc	cription	Construct universal	gates and inverte	r using M	OS and CMOS logic									
					SCHEME OF STUE	ΟY								

S. No.	Lear	ning Content	Teachir N	ng –Learning lethod	Description o Process	f T-L	Teach Hrs.	n Pract. /Tut Hrs.		LRs Re	equire	ed		Remarks
LO-14	Classific families: Saturated a logic. MOS and MOS bas input NA CM0 Two NOR	ations of logic and Non-saturated d CMOS Logic: ed NOT gate, Two ND & NOR gate. OS based NOT gate, input NAND & . gate.	Interaction lecture, f demonst assignme	ve classroom PPT, ration, quiz, ents.	Teacher will exp the contents and provide handou students. Teach will conduct qui assignments/ tu	lain d ts to er z/ torial	6		Text Hand boar	: Books douts, rd, cha	s, PPT, chalk rts.			
	1				SCHEME OF AS	SSESSI	MENT	I	1					
S. No.	Metho	od of Assessment	De	escription of A	ssessment	Max M	timum arks	R	esour	ces Re	equire	ed		External / Internal
LO-14	End Sen	nester Theory Exam	Studer 1. 2.	It will be asked Classify the lo Design univer inverter gate logic family.	to (and/or) ogic families. sal and using given		10	Ques	tion p	aper, I	Rating	scale		External
			AD	DITIONAL INS	TRUCTIONS FO	R THE I	HOD/ F	ACULTY (IF A	NY)					
	/ (Dinla	ma Wing) Ph	onal	SCHEM	E FOR LEAR	NIN	3	Branch Code	(Course Co	de	CO Code	LO Code	/
NOPV		nna wing) bi	ιυμαι	(DUTCOME			E 0 3	3	0	3	5	15	Format No. 🕂
COURS	E NAME	Digital Electronic	S											
CO Des	cription	Compare various dig	ital logic fa	amily.										
LO Des	cription	Make use of PAL & P	LA for imp	elementation of E	Boolean expression	and de	sign sim	ple logic circuit.						
					SCHEME O	F STUE	ΟY							
S. No.	Lear	ning Content	Teachir N	ng –Learning lethod	Description o Process	f T-L	Teach Hrs.	n Pract. /Tut Hrs.		LRs Re	equire	ed		Remarks

LO-15	PLD: PAL, PLA Implementation of Boolean expression using PAL, PLA (Up-to 2 variables)	Interactive classroom lecture, PPT, Video, demonstration, quiz, assignments.	Teacher will explain the contents and provide handouts to students. Teacher will conduct quiz/ assignments/ tutorial		6		Text Books, PPT, Handouts, chalk board, charts, Video lecture- NPTEL and others.	
SCHEME OF ASSESSMENT								
S. No.	Method of Assessment	Description of Assessment		Maximum Marks		Re	esources Required	External / Internal
LO-15	Seminar presentation	Student will be asked to1. Present on given PLA &/or PAL2. Implement given Boolean expression using PAL/PLA			10	Rubrics, Rating scale		Internal
ADDITIONAL INSTRUCTIONS FOR THE HOD/ FACULTY (IF ANY)								